

Model Name: 8I945GMBX

Revision 1.01

SHEET

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A94058-0

SHEET

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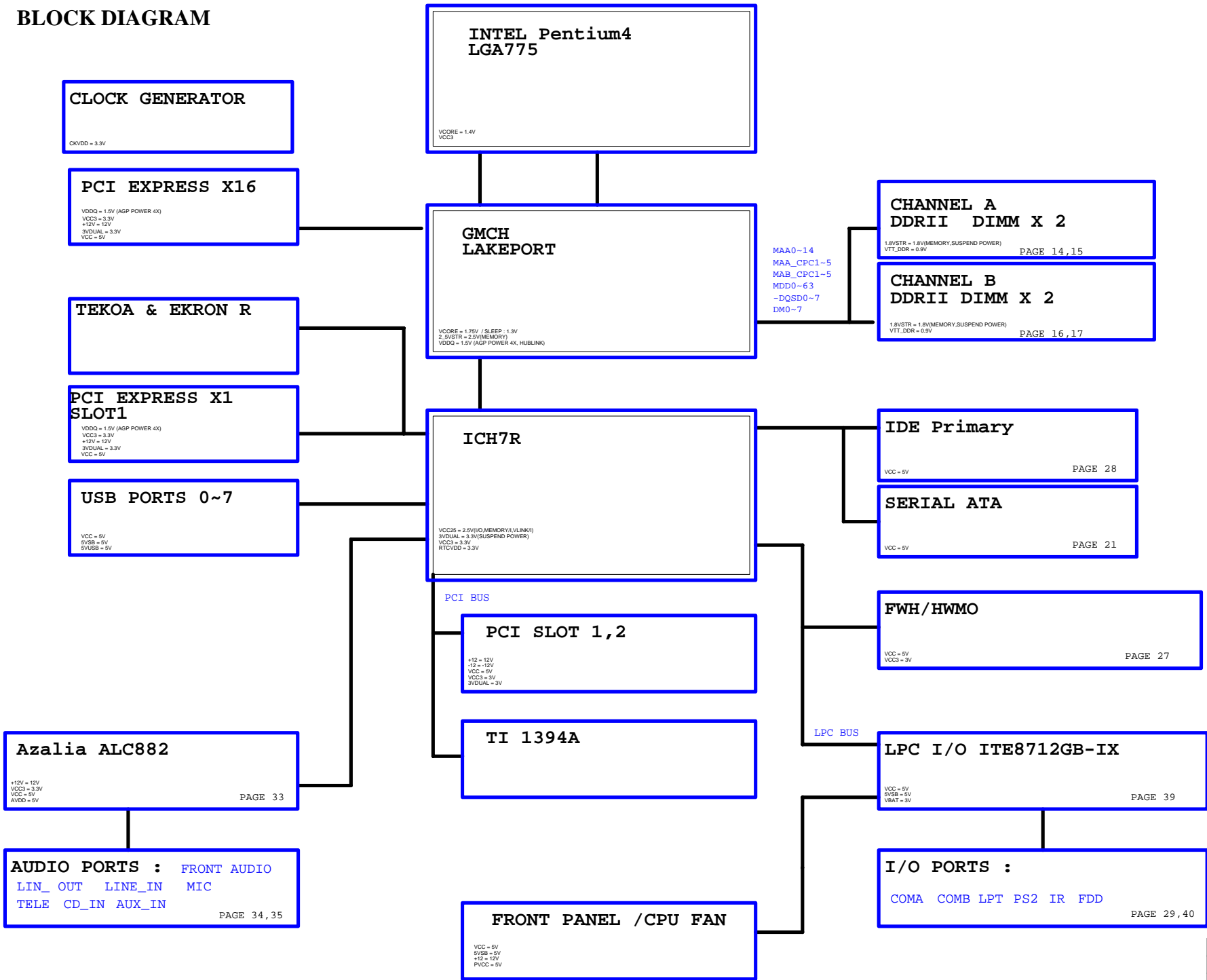
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4_LGA775_A
05	P4_LGA775_B
06	P4_LGA775_C
07	P4_LGA775_D
08	GMCH-LAKEPORT_HOST
09	GMCH-LAKEPORT_DDRII
10	GMCH-LAKEPORT_PCI E, DMI
11	GMCH-LAKEPORT_INT VGA
12	GMCH-LAKEPORT_GND
13	GMCH-LAKEPORT_PWR
14	DDRII CHANNEL A 1,2
15	DDRII CHANNEL B 1,2
16	DDRII TERMINATION
17	PCI EXPRESS*16 SLOT
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	CY28411 CKG
22	ATX,ATX_12V CONNECT,FWH BIOS
23	PCI EXPRESS*1 SLOT
24	PCI SLOT 1,2
25	H/W MONITOR,FAN
26	IDE
27	KB_PS2

28	FRONT PANEL
29	FRONT USB,REAL USB CONNECT
30	PROCESSOR HOT
31	AZALIA CODEC ALC880
32	AUDIO JACK 1
33	AUDIO JACK 2
34	TI1394A
35	TEKOA & EKRON R
36	TEKOA & EKRON R
37	ITE 8712GB
38	COM_LPT
39	VCORE PWM
40	DISCRETE POWER
41	GPIO DEFINE
42	GPIO DEFINE

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Title			Cover Sheet	
Size	Document Number	8I945GMBX		Rev
Custom				1.01
Date:	Friday, July 01, 2005	Sheet	1	of 42

BLOCK DIAGRAM



Version: 1.01

Component value change history

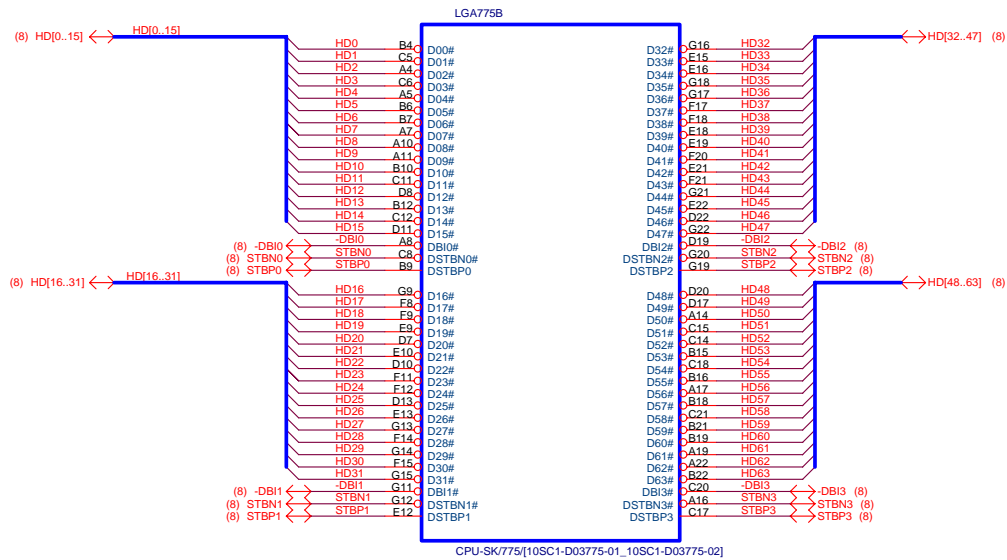
Data	Change Item	Reason
0525	Audio Jack change	*** 更換 AUDI01由 A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]變為 A3R7/13P/B/[11NR6-403007-01_11NR6-403007-02] AUDI02由 A3R7/13P/OBG/[11NR6-403006-71]變為 A3R7/13P/OBG/[11NR6-403007-51]
	VRM solution change	DC6由 33P/4/N/50V變為 180P/4/M/50V DEC1由 680U/D/4V/89變為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02] DEC12由 680U/D/4V/89變為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02] DEC23由 680U/D/4V/89變為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02] DEC6由 680U/D/4V/89變為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02] DEC9由 680U/D/4V/89變為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02] DR21由 2.87K/6/1變為 2.2K/6/1 *** 增加 BC2值為 10U/12/X/6.3V BC4值為 10U/12/X/6.3V BC6值為 10U/12/X/6.3V BC694值為 0.1U/6/Y/25V BC7值為 10U/12/X/6.3V BC711值為 0.1U/6/Y/25V DC19值為 560U/D/2.5V/8*8/[11C04-885600-01_11C04-885600-02]
	Specification change	*** 刪除 DEC20值為 680U/D/4V/89 DEC4值為 1500U/D/16V/2K DEC5值為 680U/D/4V/89 DEC7值為 680U/D/4V/89 5/[11NH2-000203-11] CU1由 ALC882/B1/S/[10HP5-366882-10]變為 ALC882/B1/S/[10HP5-366882-11] CU2由 SPT22EF340A-11-AC-52A/8變為 AS725VPS12/R/[10H4-131512-10] U26由 92573V/A3/DP4R變為 92573V/A3/10H2-400573-22R U8由 NH82801GB 1CN7/A1變為 NH82801GN 1CN7/A1/[10H41-032801-Q1R] *** 增加 BC107值為 0.1U/6/Y/25V BC108值為 0.1U/6/Y/25V EF_LED1值為 PH/1*2/BLACK EF_LED2值為 PH/1*2/BLACK IBC24值為 0.1U/6/Y/25V LBC12值為 10U/8/Y/10V LBC45值為 0.1U/6/Y/25V LBC54值為 10U/8/Y/10V LBC7值為 100U/D/10V/57 LR41值為 2.2K/6 LR60值為 0/6 LR71值為 1/6 LR72值為 1/6 LR95值為 8.2K/6 LRN10值為 10/8P4R LRN9值為 10/8P4R Q277值為 BAT54A/S Q278值為 MMBT2222A/SOT23 Q279值為 MMBT2222A/S R1645值為 0/6 R1650值為 330/6 R1651值為 330/6 R1652值為 1K/6 *** 刪除 INFO_LINK值為 H2X3/-PIN6/[11NH2-000203-31_11NH2-000203-33] LBC44值為 1U/6/Y/10V LR53值為 0/12 LR54值為 0/12 NVM_PROT值為 PH/1*2/BLACK RF_ID值為 H2X3/-PIN5/[11NH2-000203-11]
0615	Removed EF_LED1/EF_LED2	
	fixed can't boot issue	DC6 change to 33PF

Circuit or PCB layout change
for next version

[illegible]

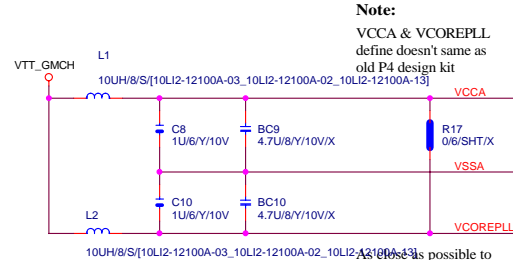
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Title			
BOM & PCB MODIFY HISTORY			
Size	Document Number		Rev
Custom	81945GMBX		1.01
Date:	Friday, July 01, 2005	Sheet	3 of 42



Note:

VCCA & VCOREPLL
define doesn't same as
old P4 design kit



Trace width doesn't
less than 12 Mil

As close as possible to
CPU socket

945 Design Guide rev1.5 spec.

VCCA=120~220mA

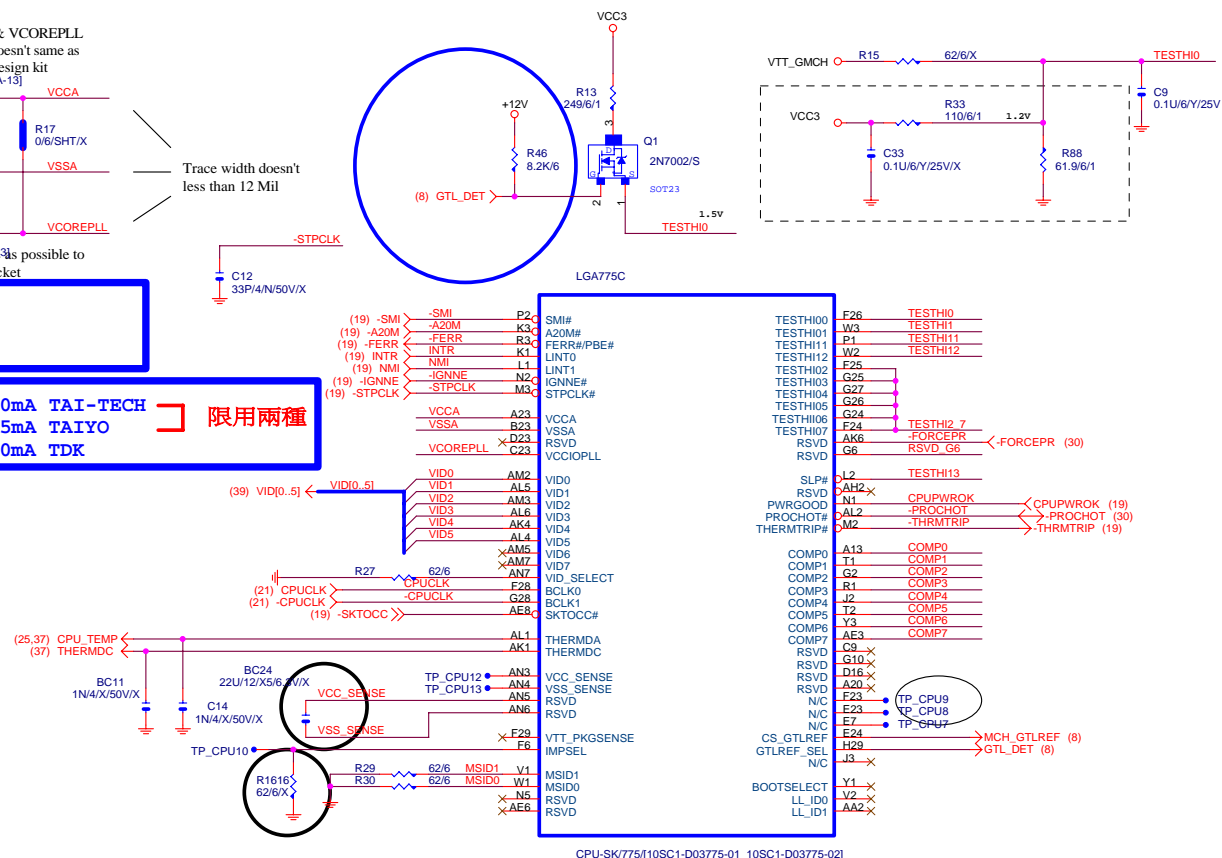
公板爲125mA

10LI2-12100A-03=INDUCTOR 10uH 300mA TAI-TECH

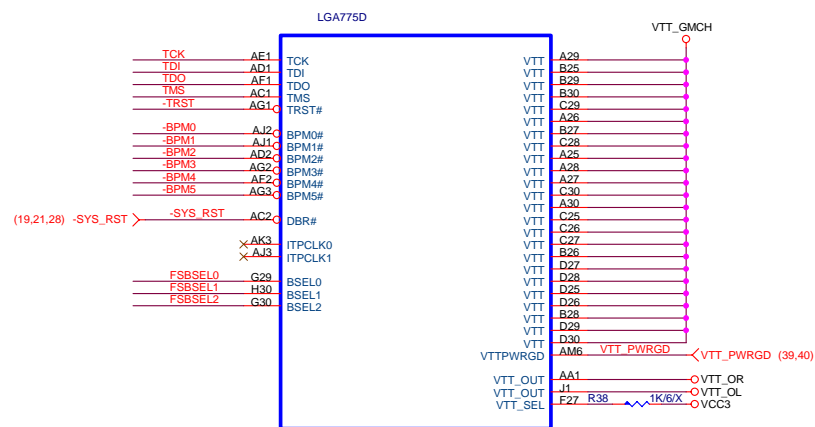
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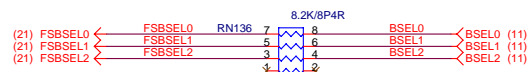
限用兩種



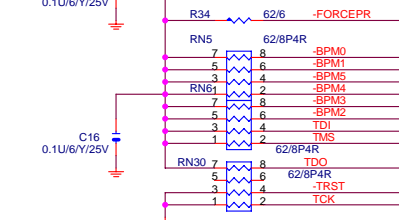
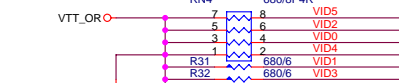
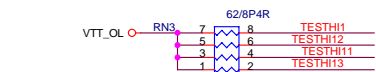
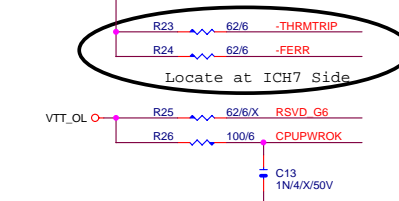
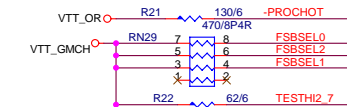
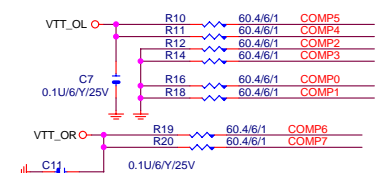
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CPU-SK/775[10SC1-D03775-01_10SC1-D03775-02]

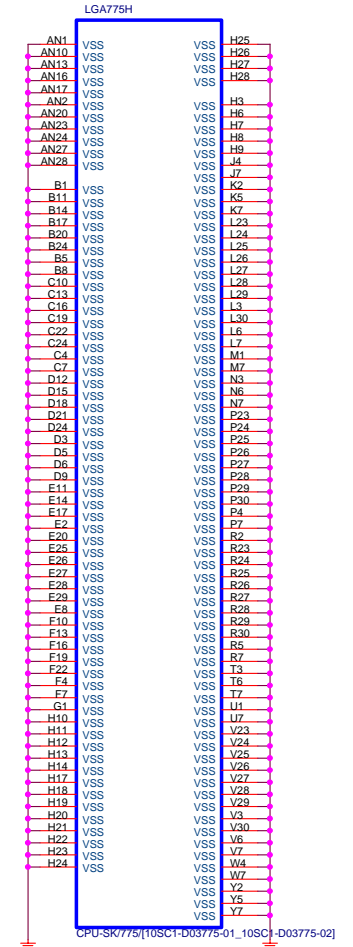
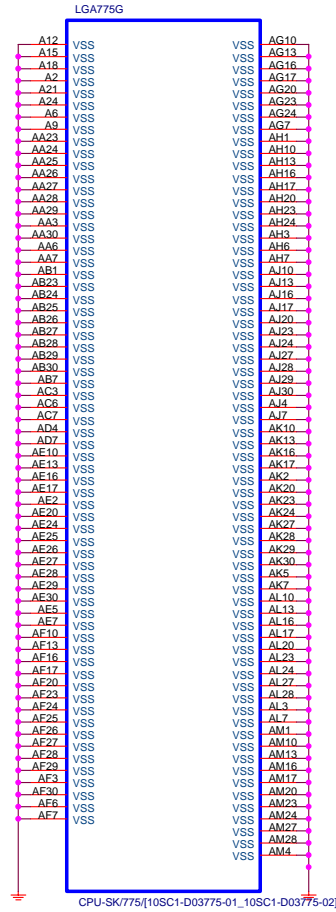
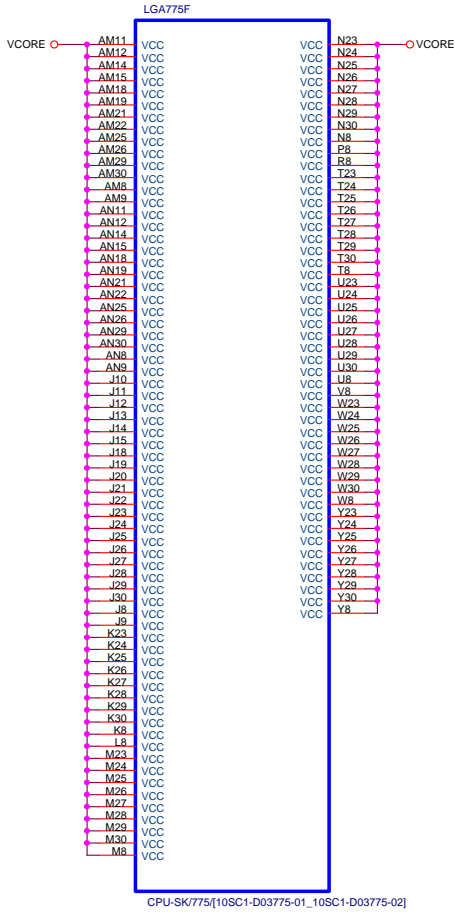
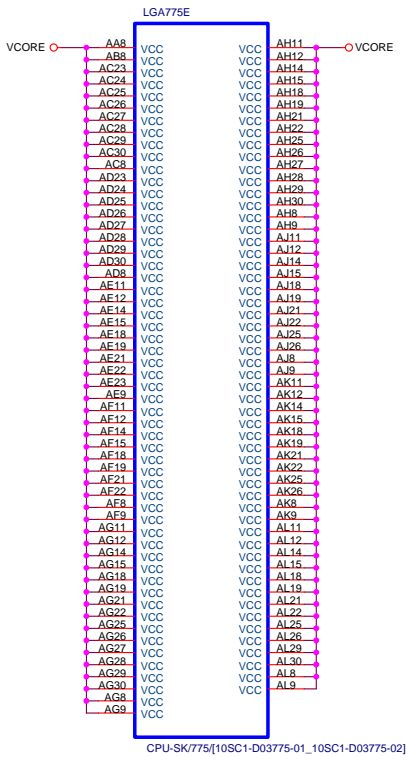


Place outside of CPU socket



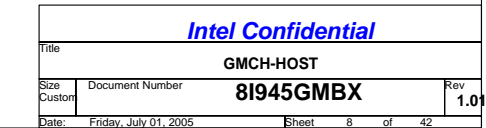
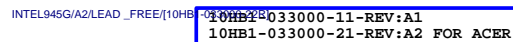
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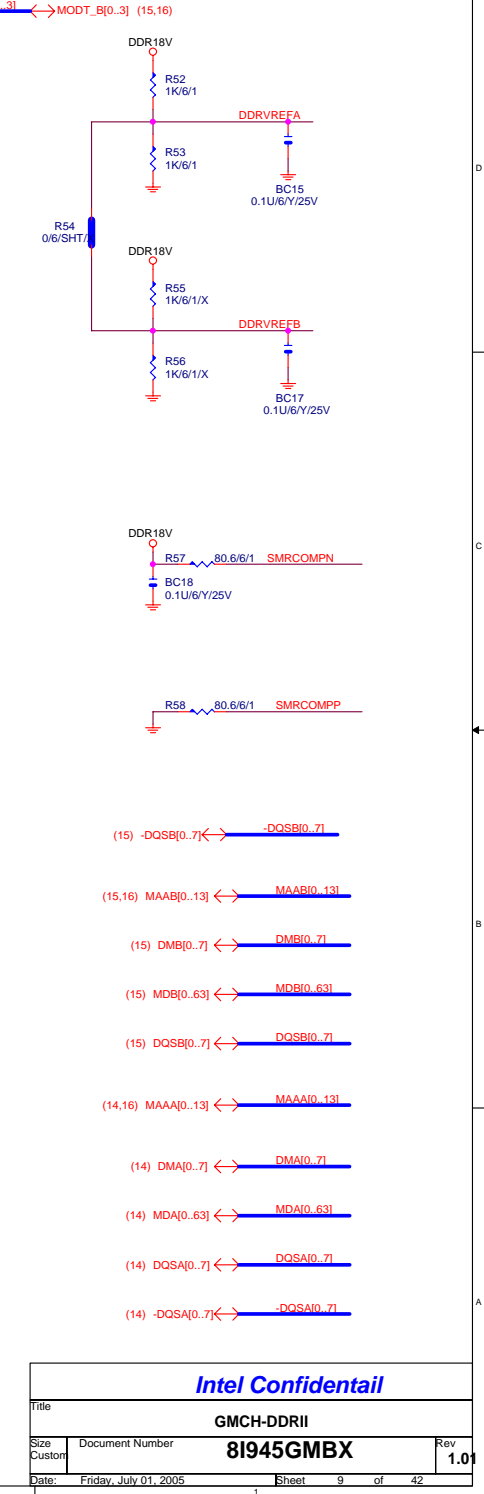
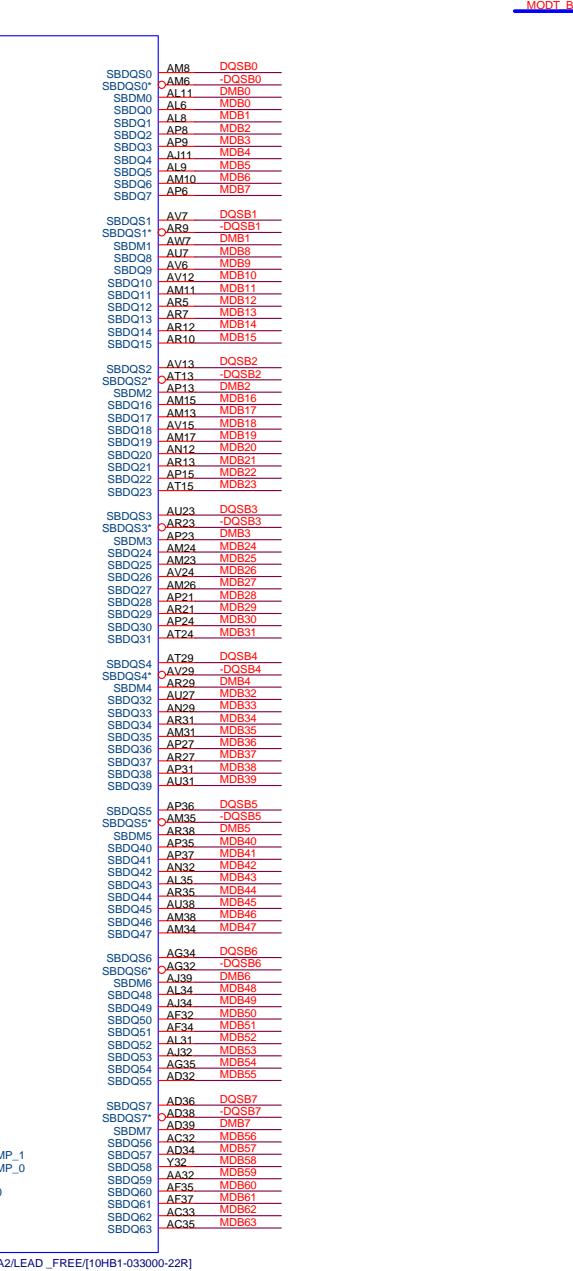
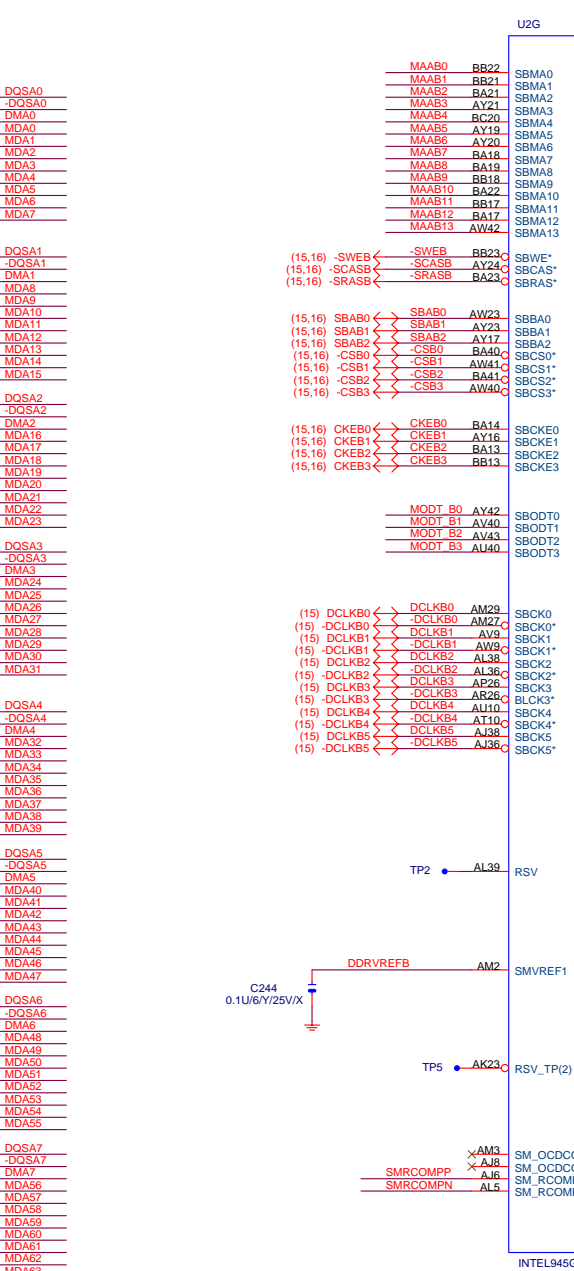
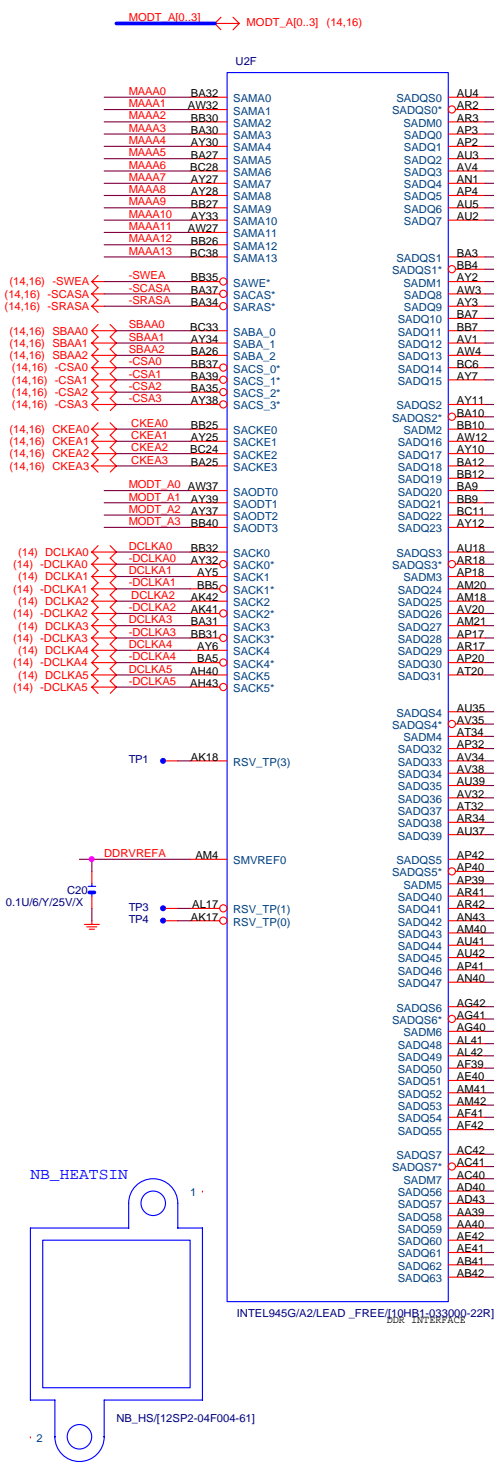
P4_LGA775-B

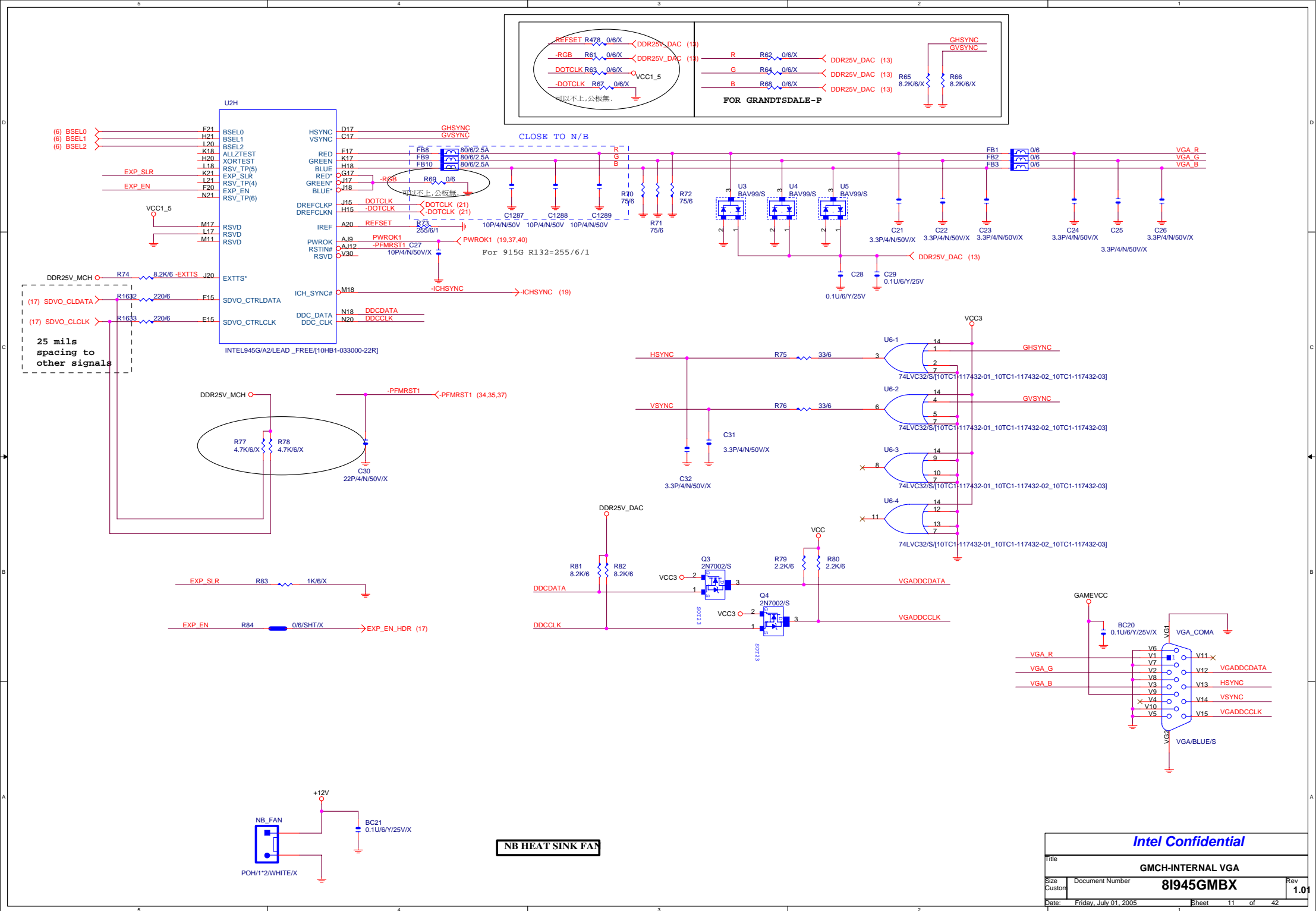


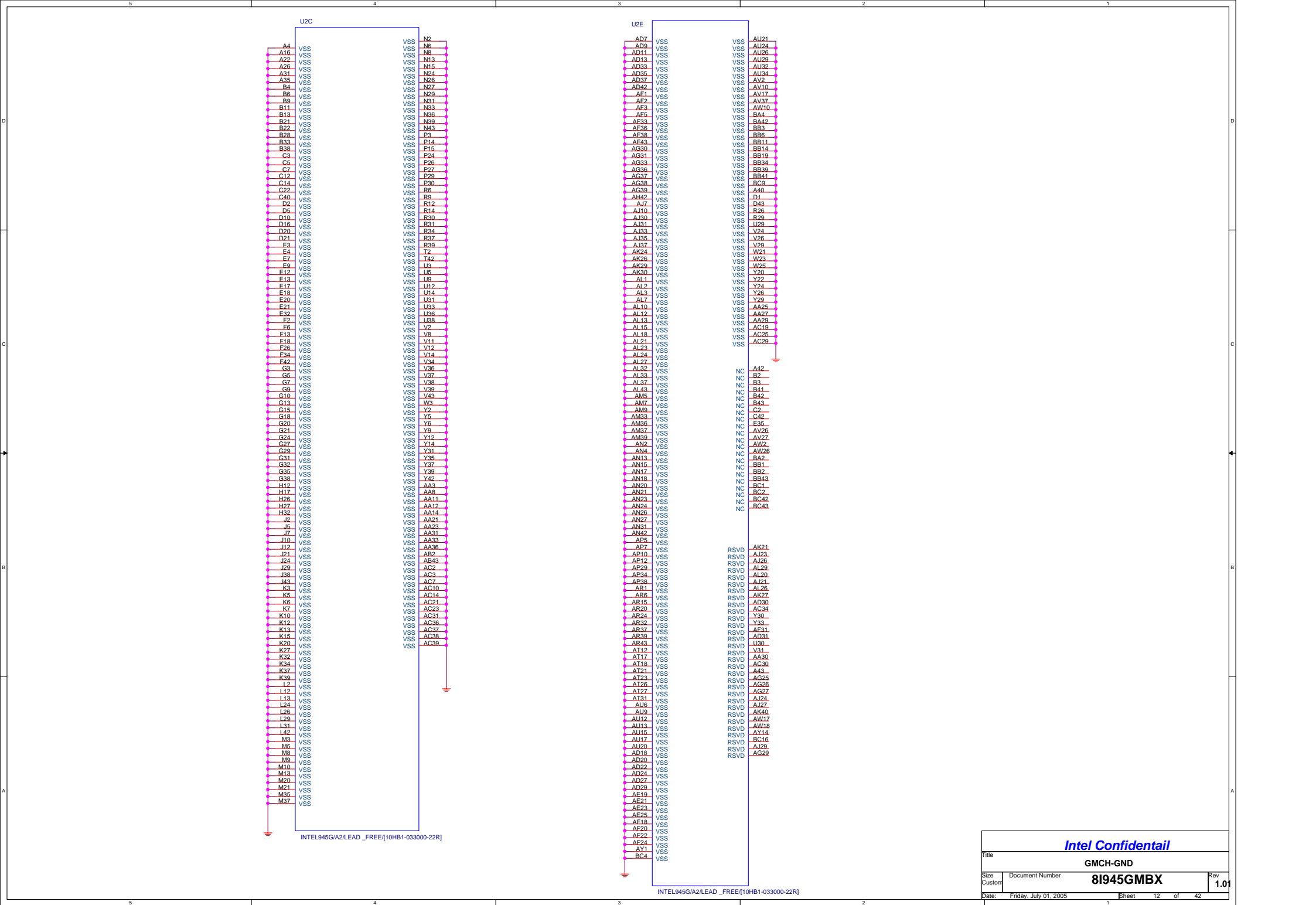
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Title		
P4_LGA775-D		
Size	Document Number	Rev
Custom	8I945GMBX	1.01
Date:	Friday, July 01, 2005	Sheet 7 of 42









1.425~1.575V

1.7~1.9V

VCC1_5

N17 VCC
P18 VCC
P20 VCC
P21 VCC
AA22 VCC
AB21 VCC
AB22 VCC
AB23 VCC
AC22 VCC
AD14 VCC
AF6 VCC
AF7 VCC
AF8 VCC
AF9 VCC
AF10 VCC
AF11 VCC
AF12 VCC
AF13 VCC
AF14 VCC
AF30 VCC
AG2 VCC
AG3 VCC
AG4 VCC
AG5 VCC
AG6 VCC
AG7 VCC
AG8 VCC
AG9 VCC
AG10 VCC
AG11 VCC
AG12 VCC
AG13 VCC
AG14 VCC
AH1 VCC
AH2 VCC
AH3 VCC
AH4 VCC
AJ5 VCC
AJ13 VCC
AJ14 VCC
AK2 VCC
AK3 VCC
AK4 VCC
AK14 VCC
AK15 VCC
AK20 VCC
R15 VCC
R17 VCC
R18 VCC
R20 VCC
R21 VCC
R23 VCC
R24 VCC

U15 VCC
U17 VCC
U18 VCC
U19 VCC
U20 VCC
U21 VCC
U22 VCC
U23 VCC
U24 VCC
U25 VCC
U26 VCC
V15 VCC
V17 VCC
V18 VCC
V19 VCC
V20 VCC
V21 VCC
V22 VCC
V23 VCC
V25 VCC
V27 VCC
W17 VCC
W18 VCC
W19 VCC
W20 VCC
W22 VCC
W24 VCC
W26 VCC
W27 VCC
Y15 VCC
Y17 VCC
Y18 VCC
Y19 VCC
Y21 VCC
Y23 VCC
Y25 VCC
Y27 VCC
AA15 VCC
AA17 VCC
AA18 VCC
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AA26 VCC
AB17 VCC
AB18 VCC
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AB20 VCC
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AB25 VCC
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AE17 VCC
AE19 VCC
AE21 VCC
AE23 VCC
AE25 VCC
AE26 VCC
AE27 VCC
AE29 VCC

VCCSM BB16
VCCSM AW15
VCCSM BB42
VCCSM BC13
VCCSM BC18
VCCSM BC22
VCCSM BC26
VCCSM BB20
VCCSM AW24
VCCSM B036
VCCSM BC31
VCCSM BB32
VCCSM BB33
VCCSM BB28
VCCSM BB24
VCCSM AW29
VCCSM AW31
VCCSM AW34
VCCSM AV41
VCCSM AV42
VCCSM AV23
VCCSM AV18
VCCSM BC40
VCCSM AW35
VCCSM AV43
VCCSM AW20
VCCSM AV21
VCCSM AW13
VCCSM AW21

VTT C23
VTT G23
VTT P23
VTT E23
VTT D23
VTT D24
VTT D25
VTT B25
VTT B24
VTT B23
VTT B26
VTT H23
VTT E23
VTT K23
VTT L23
VTT M23
VTT E24
VTT N23
VTT A24
VTT F27
VTT E27
VTT E26
VTT C25
VTT C26

VCCA_DPLL B19
VCCA_MP L B20
VCCA_MP L L C21
VCCA_HPLL C19
VCCA_DPLL A C18
VCCA_DAC D19
VCCA_DAC B17
VCCA_GPLL A18

VCC_EXP AA13
VCC_EXP AD12
VCC_EXP AC5
VCC_EXP AA5
VCC_EXP U13
VCC_EXP V5
VCC_EXP V13
VCC_EXP AE2
VCC_EXP R13
VCC_EXP N12
VCC_EXP N10
VCC_EXP R5
VCC_EXP N7
VCC_EXP N11
VCC_EXP AE3
VCC_EXP N9
VCC_EXP AD10
VCC_EXP AD1
VCC_EXP AC6
VCC_EXP AD8
VCC_EXP AD2
VCC_EXP AD4
VCC_EXP AD5
VCC_EXP AD6
VCC_EXP Y13
VCC_EXP N6
VCC_EXP U8
VCC_EXP AC13
VCC_EXP AE4
VCC_EXP U7
VCC_EXP R10
VCC_EXP U6
VCC_EXP V6
VCC_EXP V7
VCC_EXP V9
VCC_EXP V10

VCC AG15
VCC AG17
VCC AG18
VCC AG19
VCC AG20
VCC AG21
VCC AG22
VCC AG23
VCC AG24
VCC AJ15
VCC AJ17
VCC AJ18
VCC AJ20

VCCA_EXPPLL=VCCA_GPLL=45mA(1.425V~1.575V)

VCCA_HPLL>50mA 公板爲200mA(1.425V~1.575V)

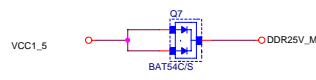
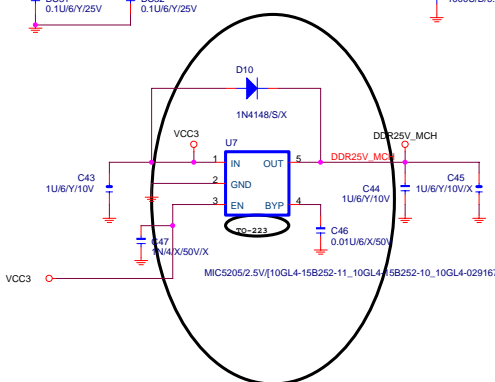
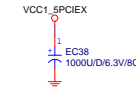
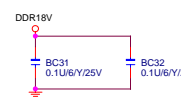
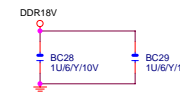
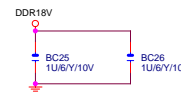
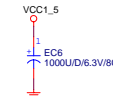
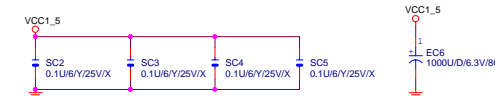
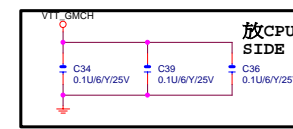
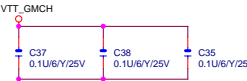
VCCA_DPLL A=65mA(1.425V~1.575V)

VCCA_DPLL B=65mA(1.425V~1.575V)

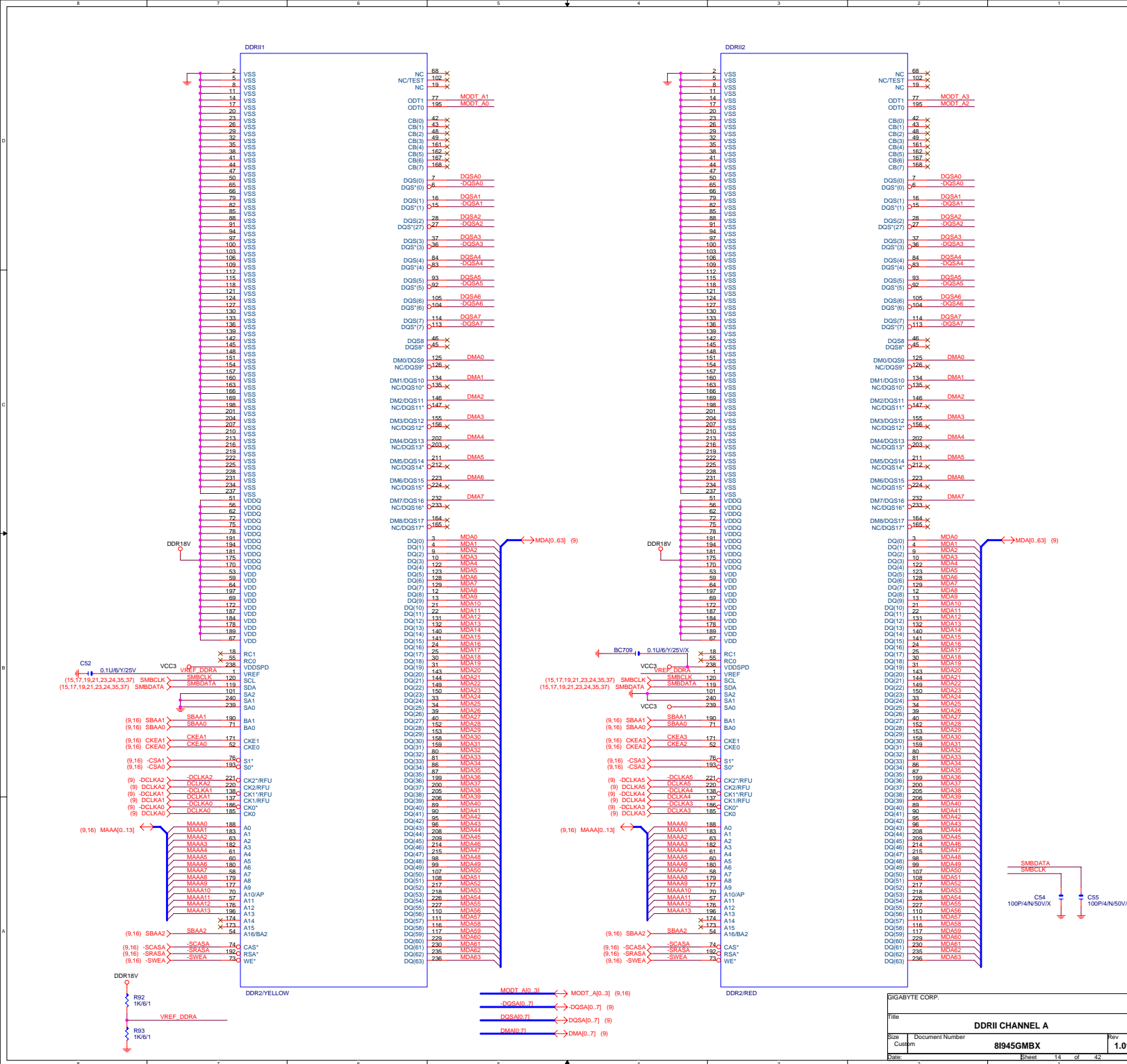
VCCA_MPLL>50mA(1.425V~1.575V)

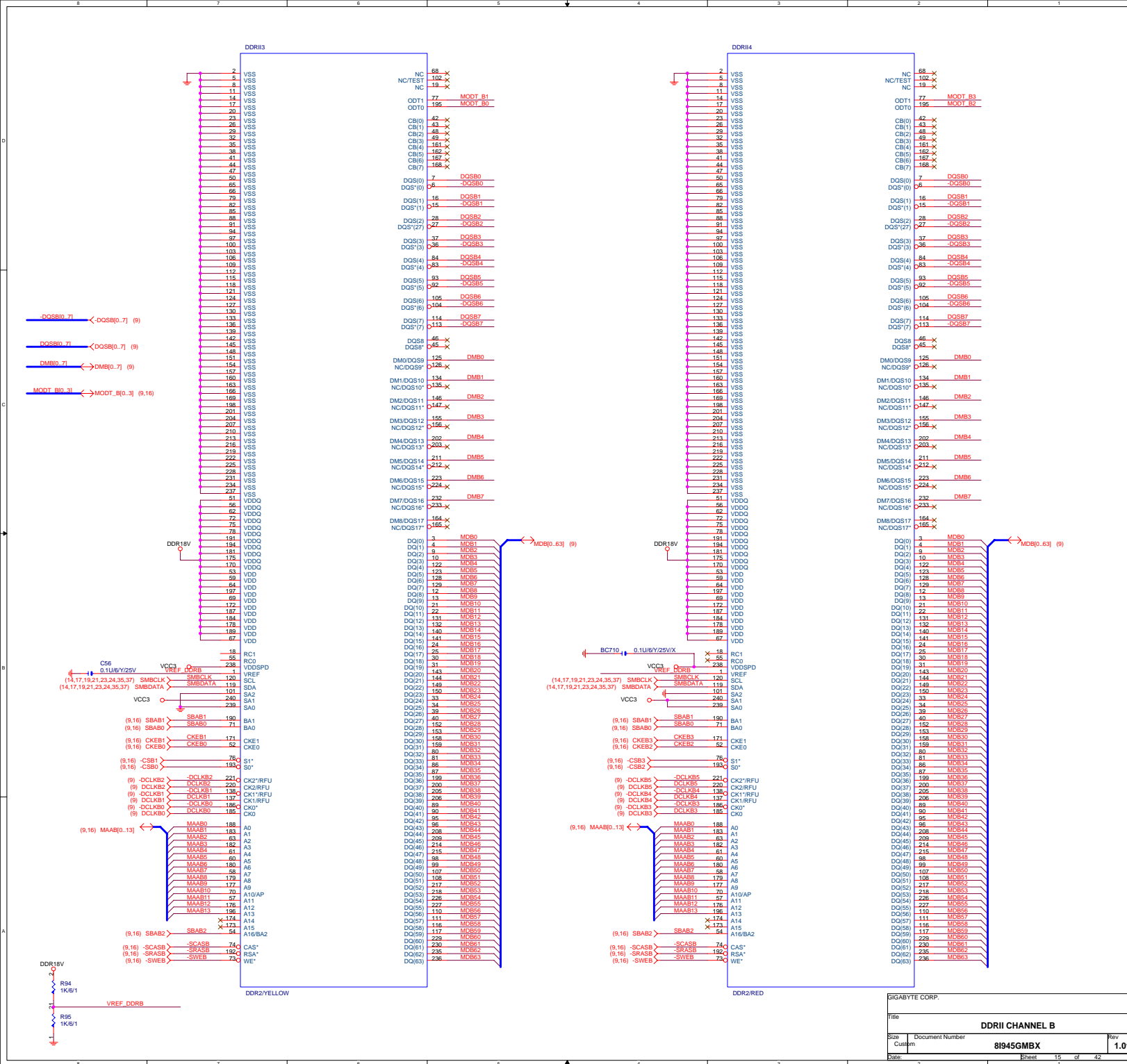
VCCA_DAC=DDR25V_DAC=70mA(2.375~2.625V)

945 Design Guide rev1.5 spec.
VCCA_EXPPLL=VCCA_GPLL=45mA(1.425V~1.575V)
VCCA_HPLL>50mA 公板爲200mA(1.425V~1.575V)
VCCA_DPLL A=65mA(1.425V~1.575V)
VCCA_DPLL B=65mA(1.425V~1.575V)
VCCA_MPLL>50mA(1.425V~1.575V)
VCCA_DAC=DDR25V_DAC=70mA(2.375~2.625V)

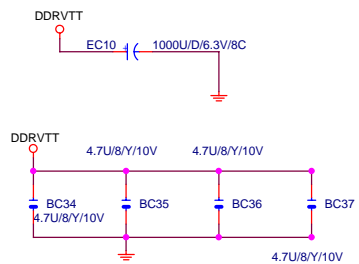


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File	GMCH-PWR		
Size	Document Number	8I945GMBX	Rev
Custom			1.01
Date	Friday, July 01, 2005	Sheet	13 of 42

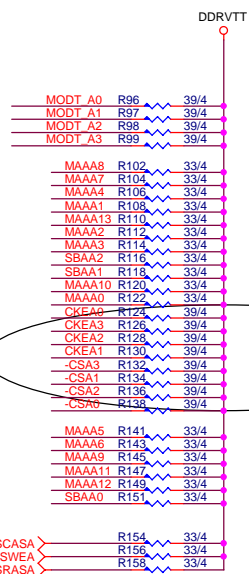
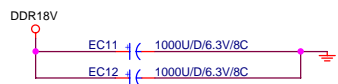




DDRVTT Decouple

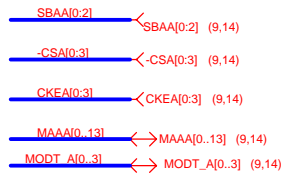
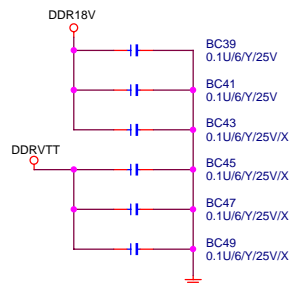


DDR TERMINATION CHANNEL A

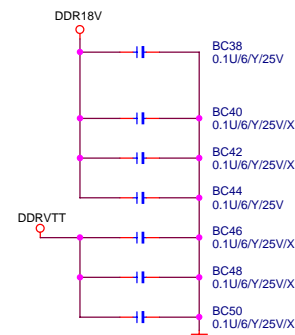


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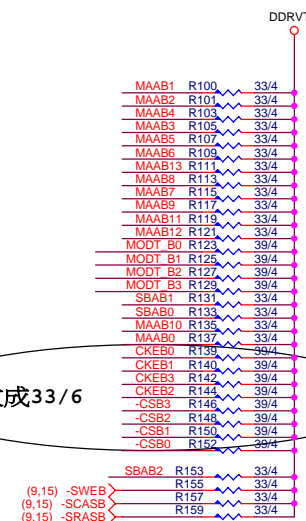
DDR18V Decouple



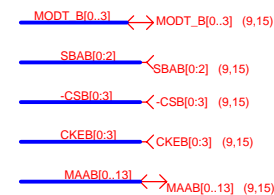
DDR18V Decouple

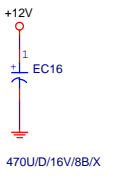
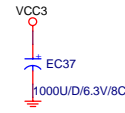


CHANNEL B



全部改成33/6



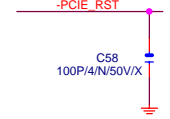
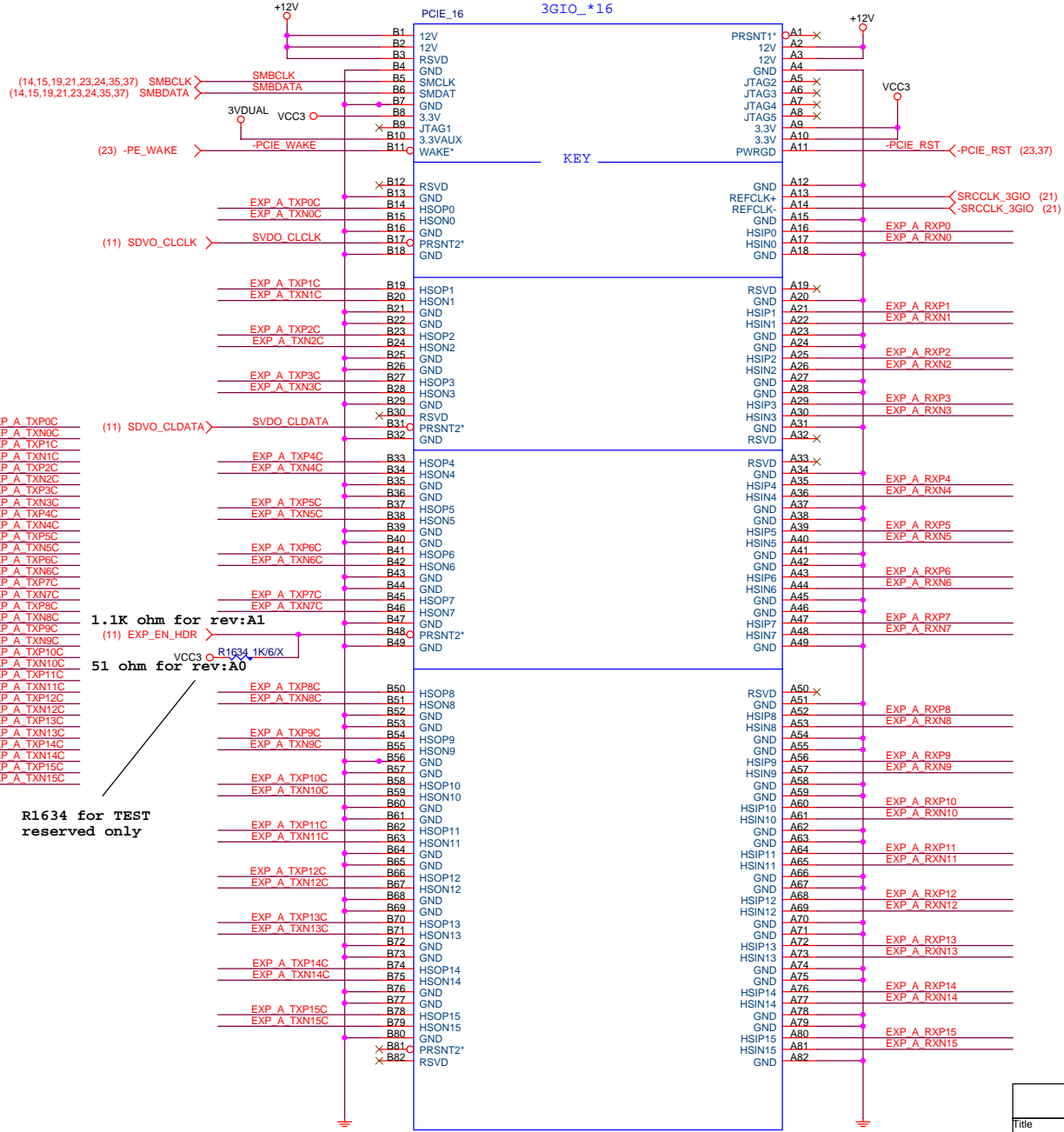


EXP_A_TXP[0..15] >>> EXP_A_TXP[0..15] (10)
EXP_A_TXN[0..15] >>> EXP_A_TXN[0..15] (10)

EXP_A_TXP0	C59	0.1u/6V/25V	EXP_A_TXP0C
EXP_A_TXN0	C60	0.1u/6V/25V	EXP_A_TXN0C
EXP_A_TXP1	C61	0.1u/6V/25V	EXP_A_TXP1C
EXP_A_TXN1	C62	0.1u/6V/25V	EXP_A_TXN1C
EXP_A_TXP2	C63	0.1u/6V/25V	EXP_A_TXP2C
EXP_A_TXN2	C64	0.1u/6V/25V	EXP_A_TXN2C
EXP_A_TXP3	C65	0.1u/6V/25V	EXP_A_TXP3C
EXP_A_TXN3	C66	0.1u/6V/25V	EXP_A_TXN3C
EXP_A_TXP4	C67	0.1u/6V/25V	EXP_A_TXP4C
EXP_A_TXN4	C68	0.1u/6V/25V	EXP_A_TXN4C
EXP_A_TXP5	C69	0.1u/6V/25V	EXP_A_TXP5C
EXP_A_TXN5	C70	0.1u/6V/25V	EXP_A_TXN5C
EXP_A_TXP6	C71	0.1u/6V/25V	EXP_A_TXP6C
EXP_A_TXN6	C72	0.1u/6V/25V	EXP_A_TXN6C
EXP_A_TXP7	C73	0.1u/6V/25V	EXP_A_TXP7C
EXP_A_TXN7	C74	0.1u/6V/25V	EXP_A_TXN7C
EXP_A_TXP8	C75	0.1u/6V/25V	EXP_A_TXP8C
EXP_A_TXN8	C76	0.1u/6V/25V	EXP_A_TXN8C
EXP_A_TXP9	C77	0.1u/6V/25V	EXP_A_TXP9C
EXP_A_TXN9	C78	0.1u/6V/25V	EXP_A_TXN9C
EXP_A_TXP10	C79	0.1u/6V/25V	EXP_A_TXP10C
EXP_A_TXN10	C80	0.1u/6V/25V	EXP_A_TXN10C
EXP_A_TXP11	C81	0.1u/6V/25V	EXP_A_TXP11C
EXP_A_TXN11	C82	0.1u/6V/25V	EXP_A_TXN11C
EXP_A_TXP12	C83	0.1u/6V/25V	EXP_A_TXP12C
EXP_A_TXN12	C84	0.1u/6V/25V	EXP_A_TXN12C
EXP_A_TXP13	C85	0.1u/6V/25V	EXP_A_TXP13C
EXP_A_TXN13	C86	0.1u/6V/25V	EXP_A_TXN13C
EXP_A_TXP14	C87	0.1u/6V/25V	EXP_A_TXP14C
EXP_A_TXN14	C88	0.1u/6V/25V	EXP_A_TXN14C
EXP_A_TXP15	C89	0.1u/6V/25V	EXP_A_TXP15C
EXP_A_TXN15	C90	0.1u/6V/25V	EXP_A_TXN15C

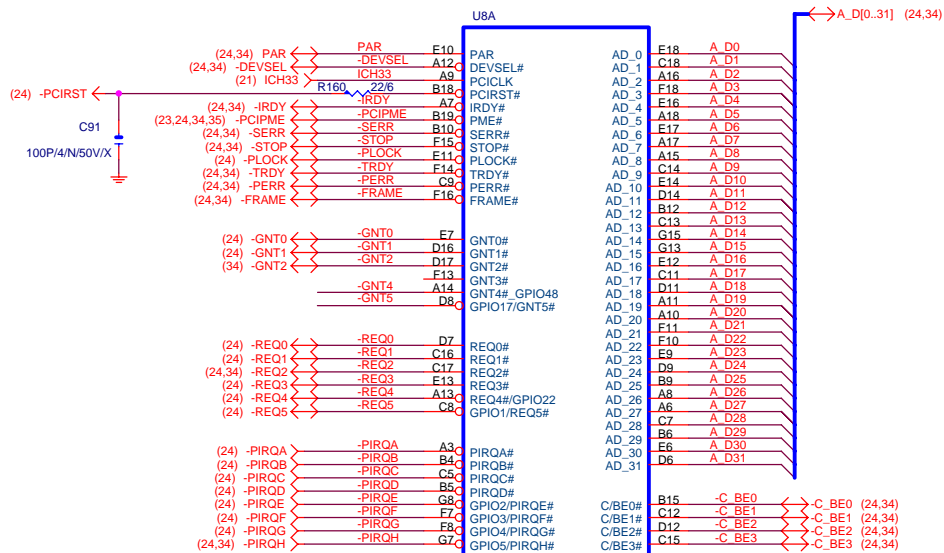
1.1K ohm for rev:A1
(11) EXP_EN_HDR
51 ohm for rev:A0

R1634 for TEST reserved only

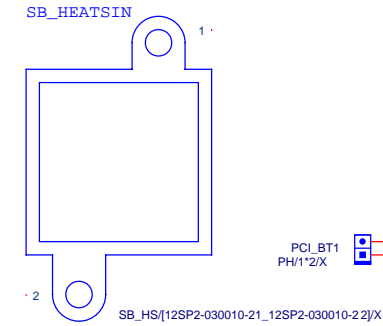


EXP_A_RXP[0..15] >>> EXP_A_RXP[0..15] (10)
EXP_A_RXN[0..15] >>> EXP_A_RXN[0..15] (10)

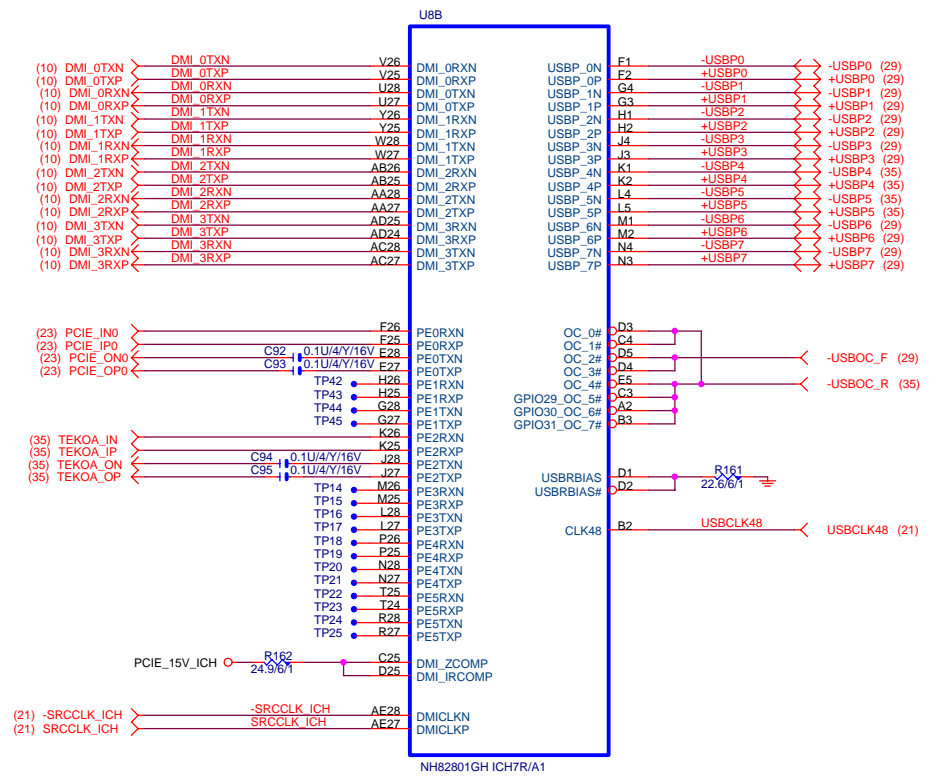
PCI-E16[11AC1-021164-61]

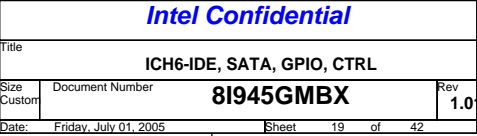


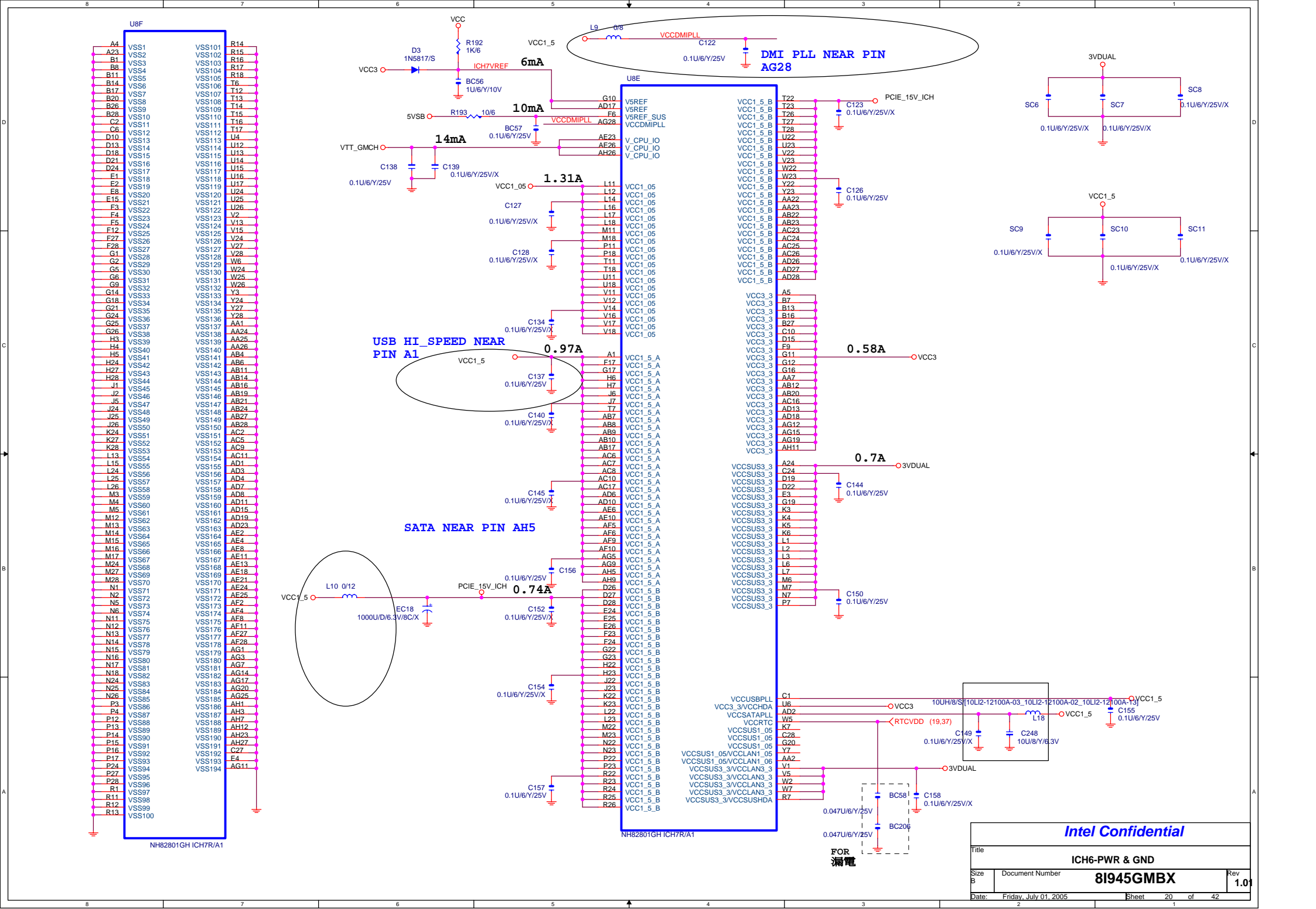
10HB1-032801-M1 REV:NON

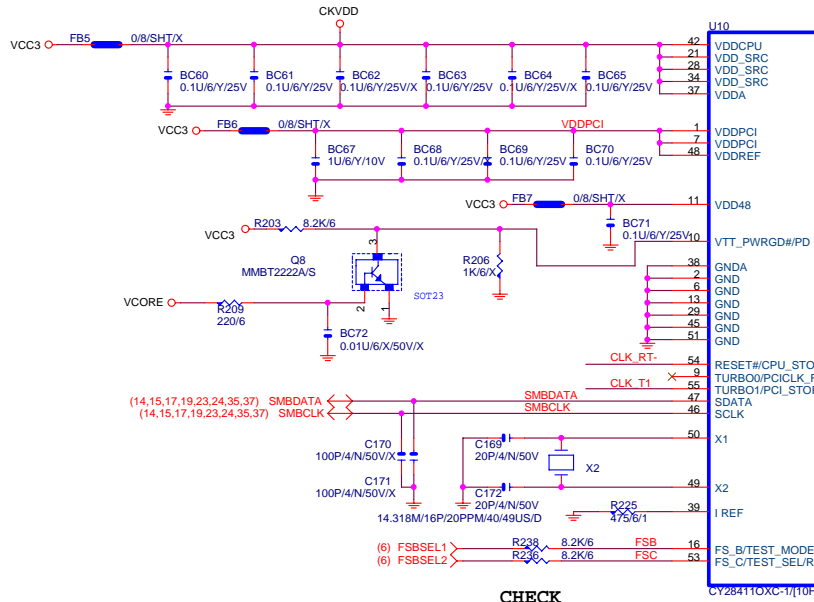


PCI_BT2: OPEN FWH
CLOSE SPI



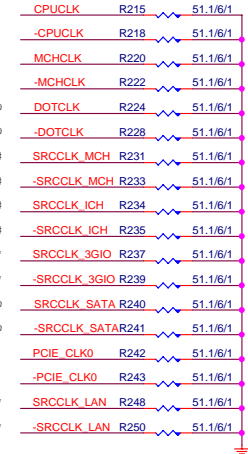
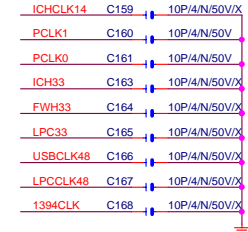
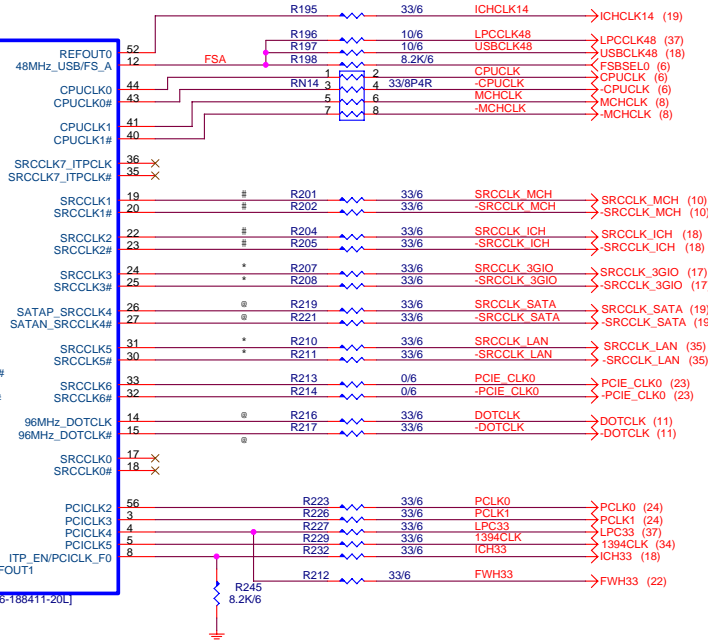
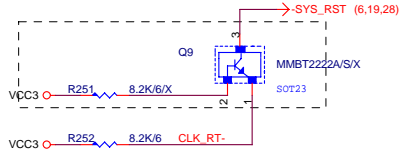






CHECK
14.318M
COUNTER

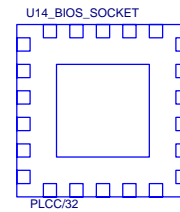
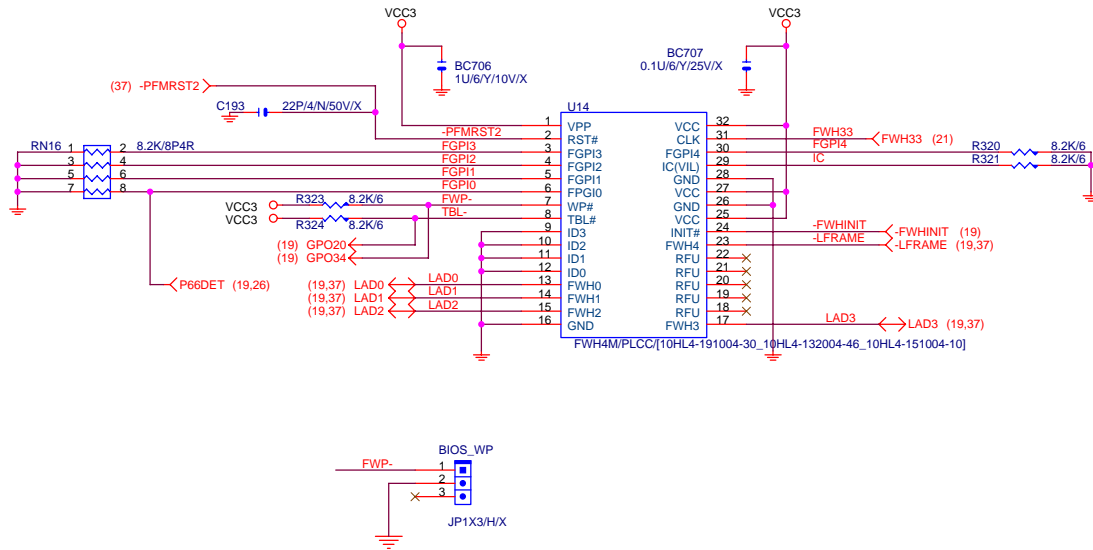
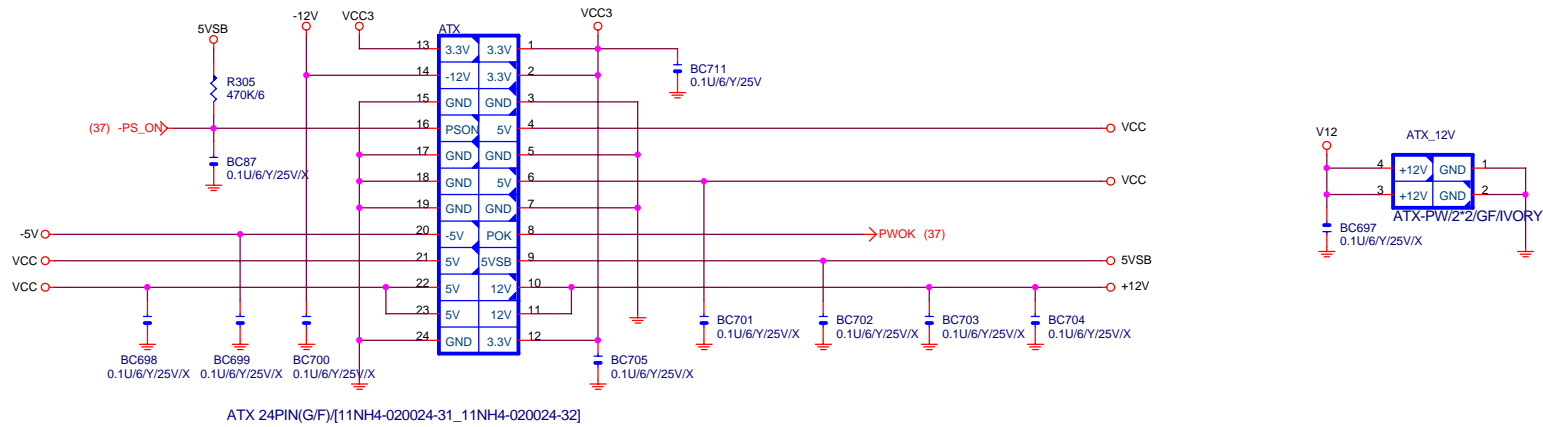
CY284110XC-1無RESET,不可上Q53,否則CPU_STOP#產生,造成CPURST- DELAY 200ms (spec>1ms)



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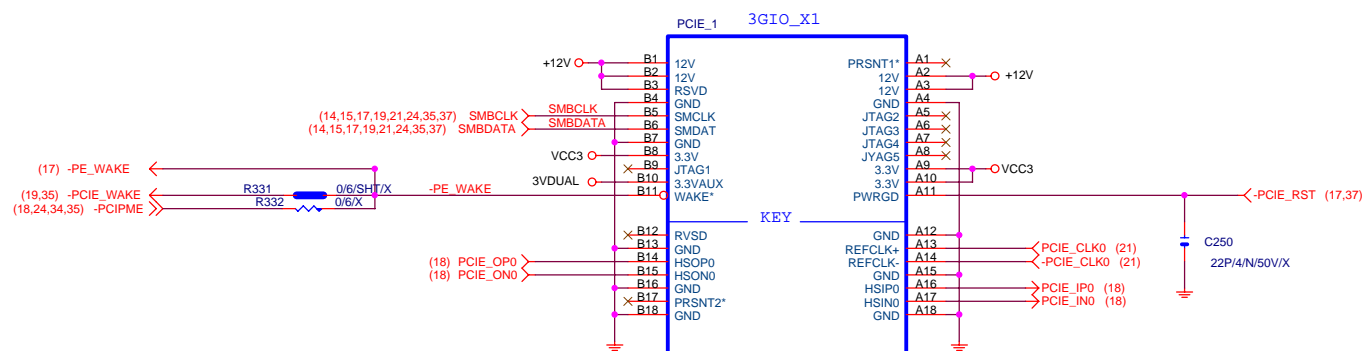
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ICS954148AF			
Size			
Custom			
Document Number			
81945GMBX			
Date:			
Friday, July 01, 2005			
Sheet			
21 of 42			
Rev			
1.01			

ATX POWER CONNECTOR

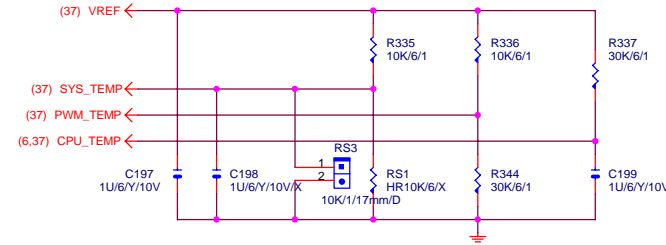


GIGABYTE

Title			
ATX POWER CONNECTOR,DUAL BIOS			
Size	Document Number	8I945GMBX	Rev
B			1.01
Date:	Friday, July 01, 2005	Sheet	22 of 42
	2		1



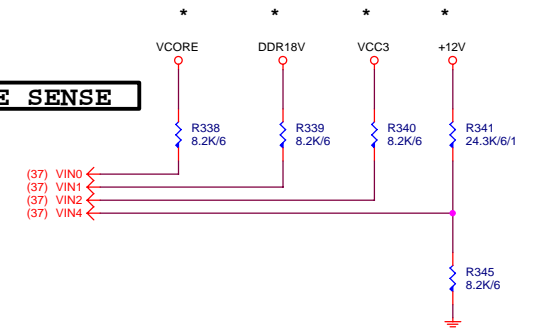
TEMP. SENSE



RS3 CLOSE TO MCH, CO-LAYOUT WITH RS1



VOLTAGE SENSE



CPU/SYS FAN

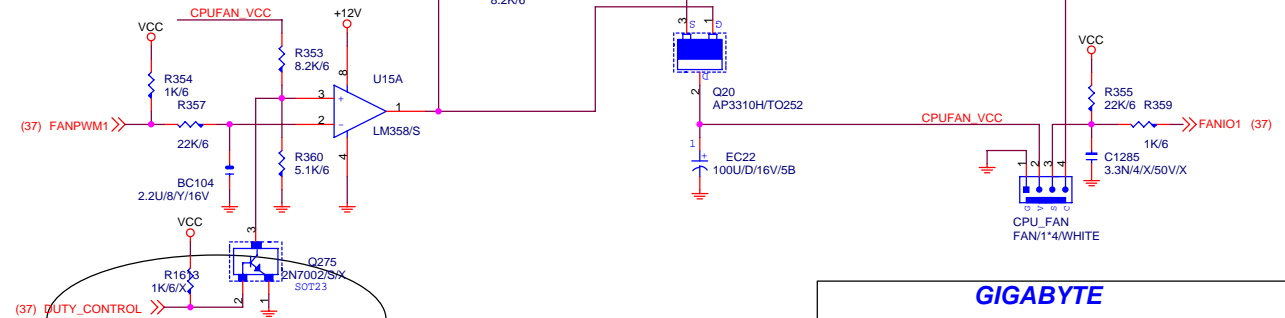
If use PBSS5240 lpcs : (non airflow)

CPUFAN_VCC=12V: Temp=40 deg
 CPUFAN_VCC=11V: Temp=82 deg
 CPUFAN_VCC=10V: Temp=70 deg
 CPUFAN_VCC= 9V: Temp=110 deg
 CPUFAN_VCC= 8V: Temp>200 deg

If use PBSS5240 lpcs : (with airflow)

CPUFAN_VCC=12V: Temp=33 deg
 CPUFAN_VCC=11V: Temp=62 deg
 CPUFAN_VCC=10V: Temp=86 deg
 CPUFAN_VCC= 9V: Temp=117 deg
 CPUFAN_VCC= 8V: Temp>122 deg

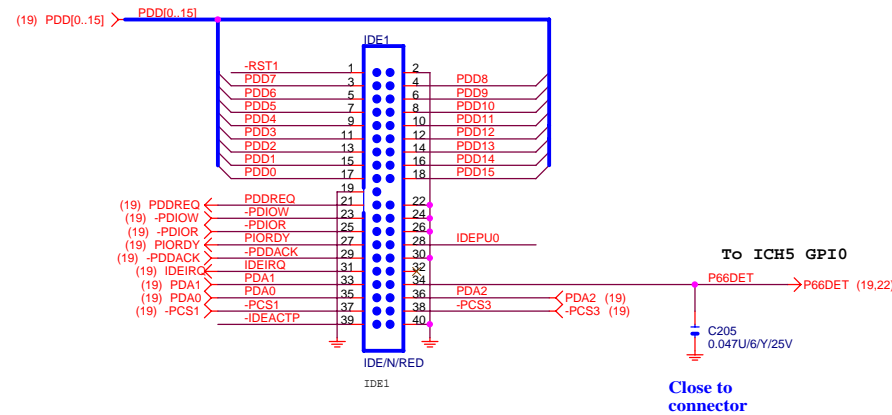
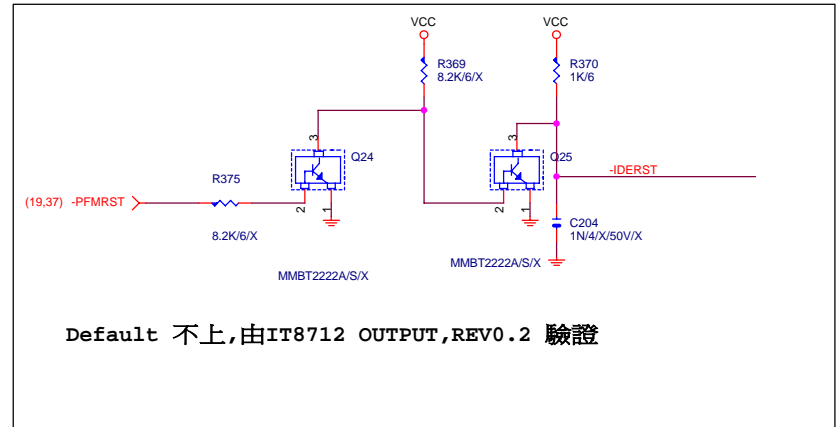
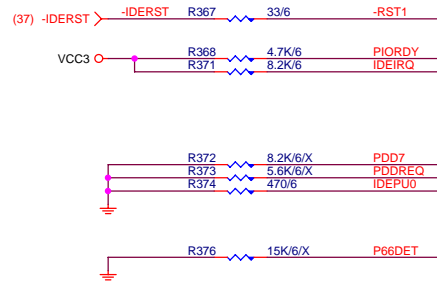
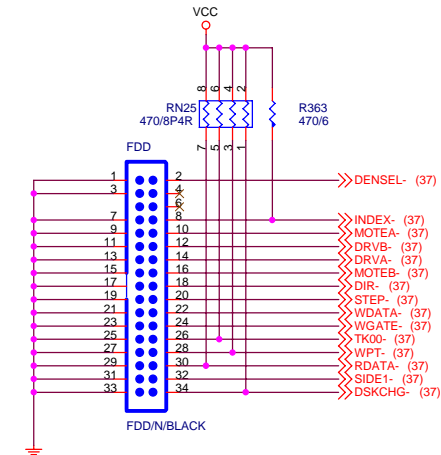
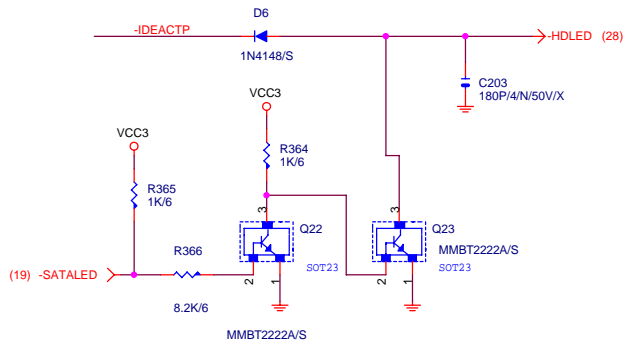
ThermalTake FAN Power Consumption: 0.82A
 Intel FAN Power Consumption Spec: 1.1A



default is high
 gpiox pin 可以3.3v or 5v
 if 3pin fan 則開機後將 program is low

GIGABYTE

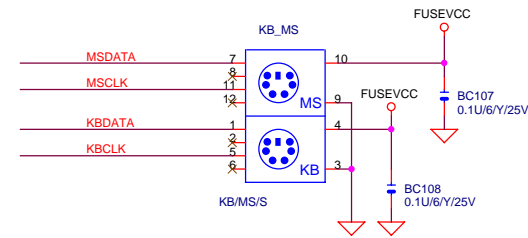
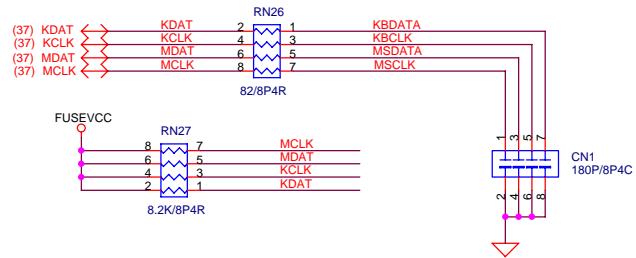
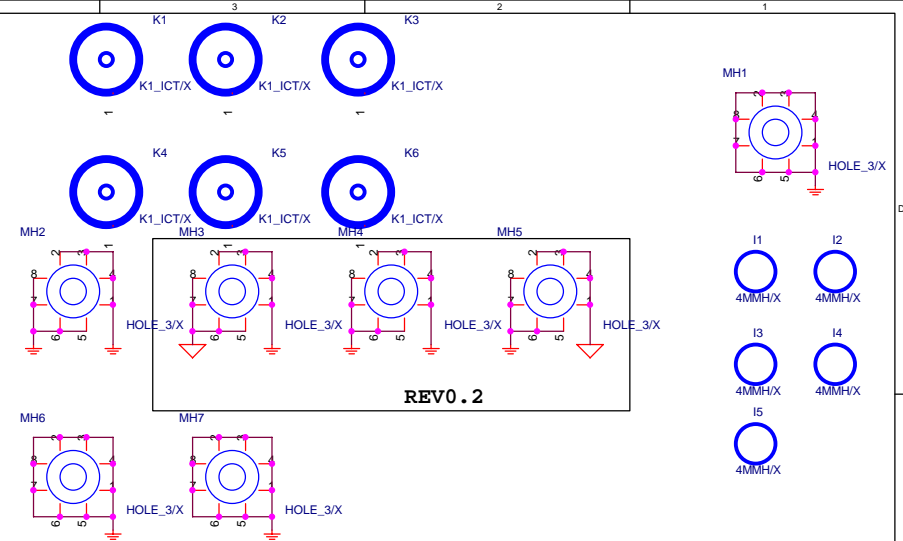
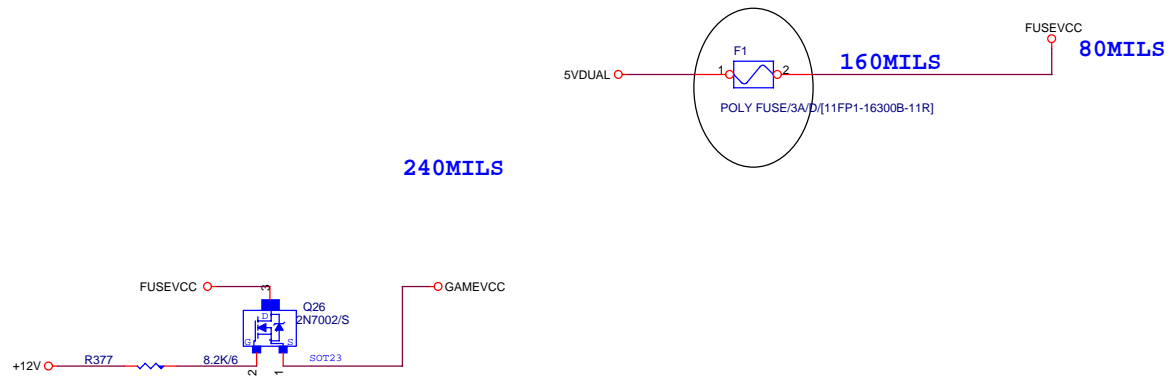
Title		
HWM/FAN/C/BIOS		
Size	Document Number	Rev
Custom	8I945GMBX	1.01
Date:	Friday, July 01, 2005	Sheet 25 of 42



PRIMARY IDE CONNECTOR

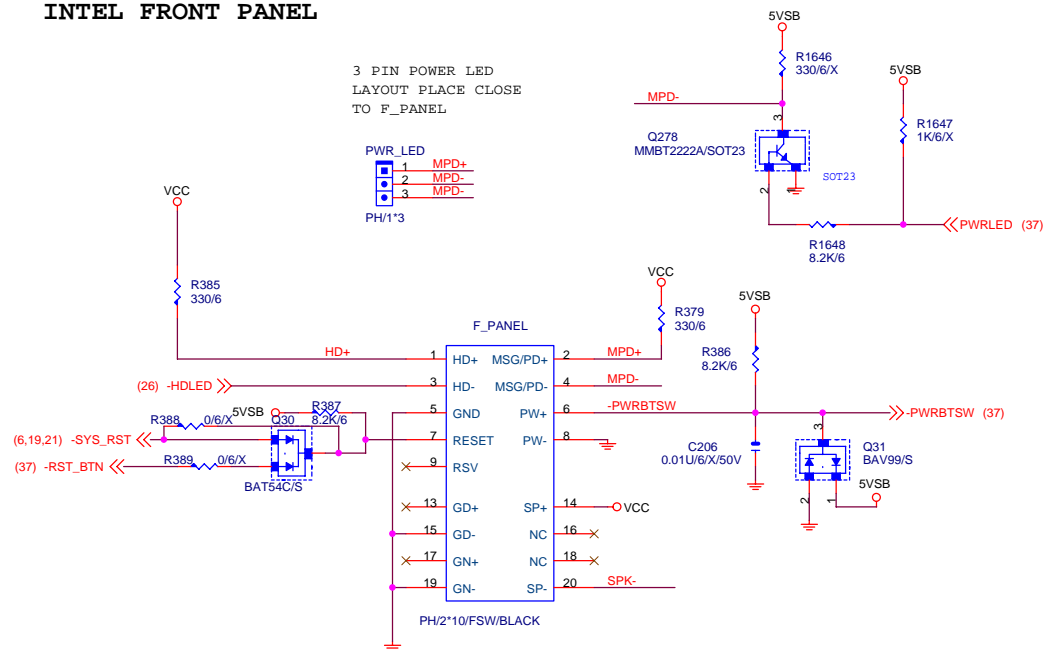
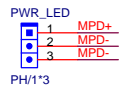
Intel Confidential

Title			IDE	
Size			8I945GMBX	
Date:			Friday, July 01, 2005	
Sheet			26 of 42	
Rev			1.01	

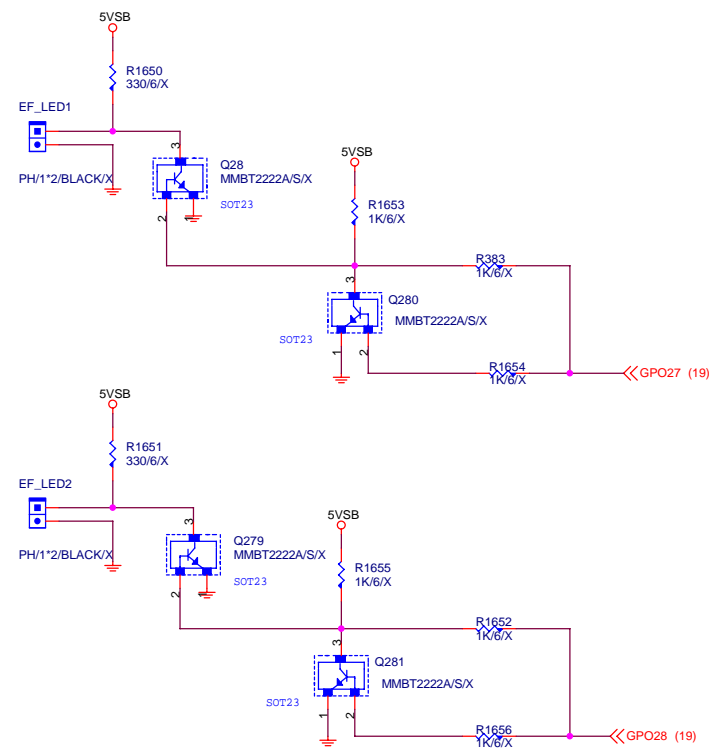
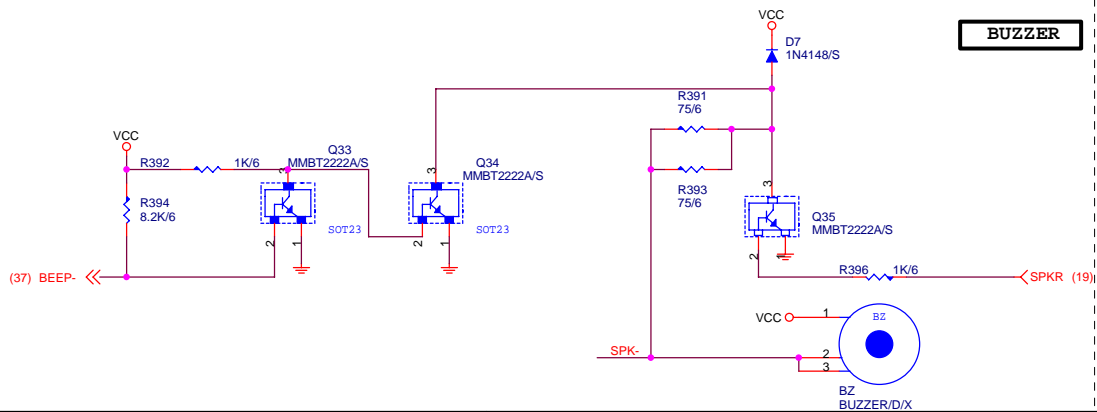


INTEL FRONT PANEL

3 PIN POWER LED
LAYOUT PLACE CLOSE
TO F_PANEL



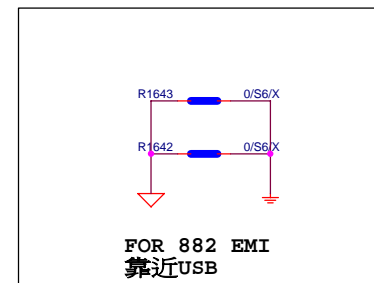
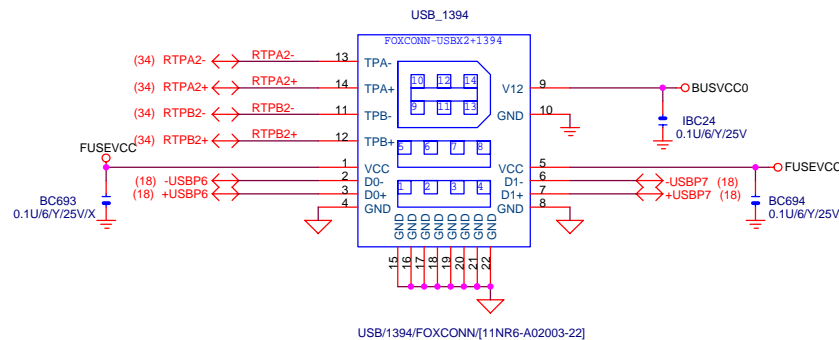
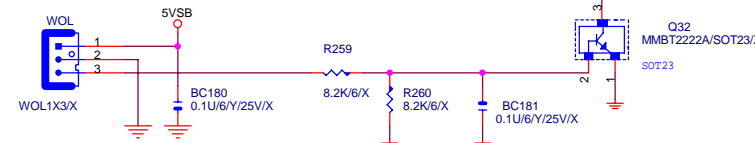
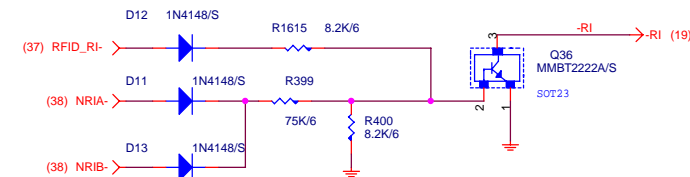
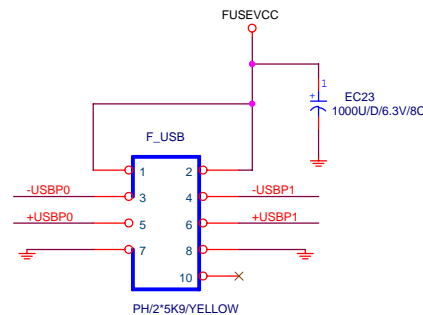
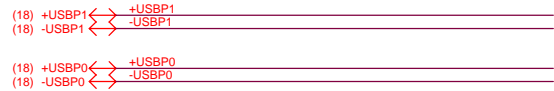
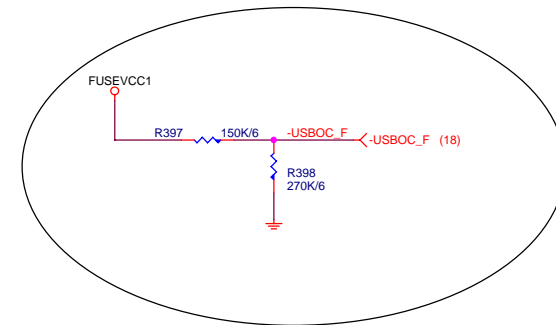
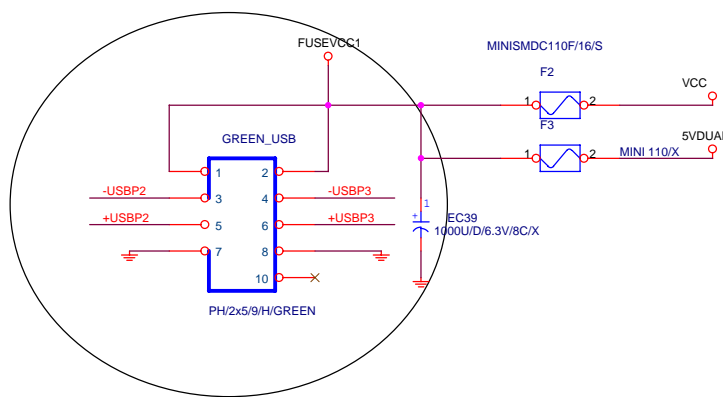
BUZZER



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<i>Intel Confidential</i>			
Title			
FRONT PANEL			
Size Custom	Document Number	81945GMBX	Rev 1.01
Date:	Friday, July 01, 2005	Sheet 28 of 42	

FRONT USB



RS2 CLOSE CPU VR MOSFET

+12V

R401 10K/6/1

R402 10K/6/1

R403 619/6/1

R404 680/6/X

U15B LM358/S

Q37 2N7002/S SOT23

Q38 2N7002/S SOT23

C208 0.1U/6V/25V

TSM 5

TSM 6

TSM 7

RS2 10RH2-001003-2

100K/1/6/S/[10RH2-001003-2]

請加替料

Place at PH4 copper

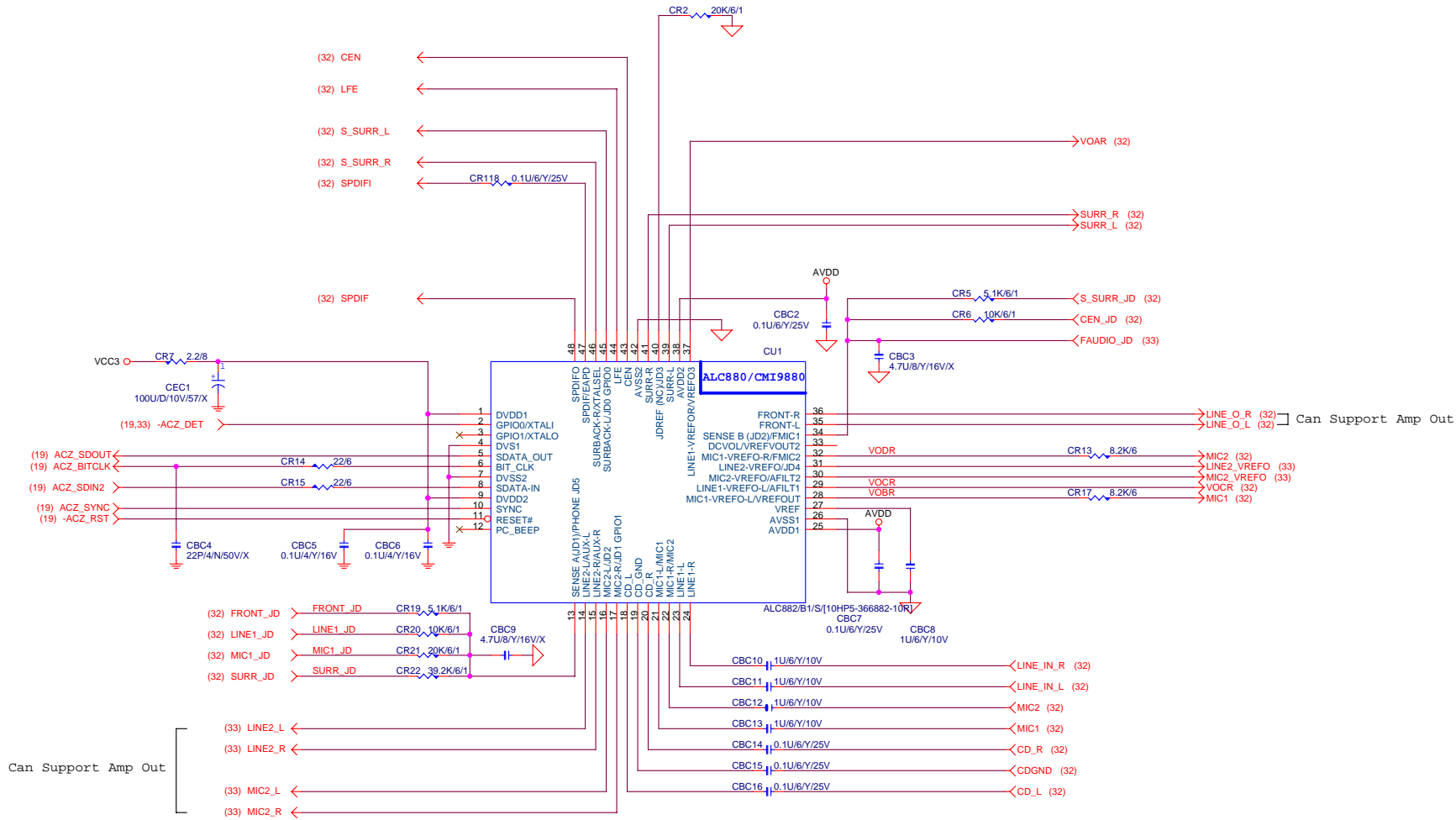
-PROCHOT (6)

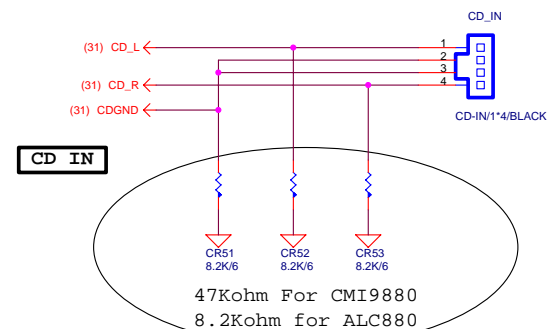
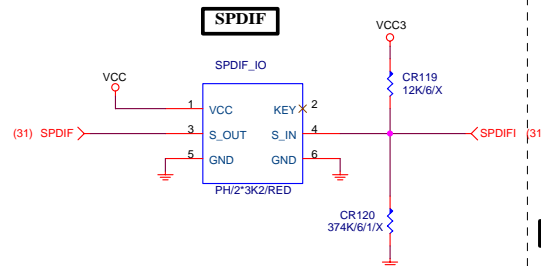
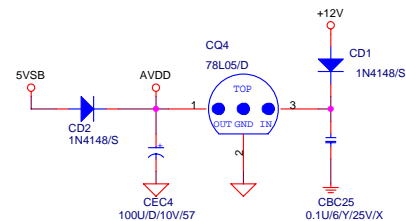
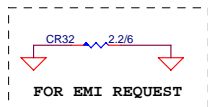
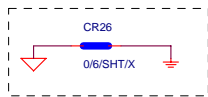
PRESCOTT

-FORCEPR (6)

The schematic diagram illustrates the fan speed control circuit. It features two LM358 op-amp comparators, U25A and U25B. U25A's non-inverting input (+) is connected to a voltage divider consisting of R1621 (8.2K/6/X) and R1626 (5.1K/6/1/X) across a +12V supply. Its inverting input (-) is connected to the FANPWM2 signal (37) through R1623 (1K/6/X) and R1624 (22K/6/X). A BC708 diode (2.2U/8/Y/16V/X) is connected between the inputs. The output of U25A (pin 1) drives the base of a PNP transistor Q276 (AP3310H/TO252/X), which controls the SYS_FAN motor. U25B's non-inverting input (+) is connected to a voltage divider consisting of R1625 (22K/6) and R1627 (1K/6) across a +12V supply. Its inverting input (-) is connected to the FANIO2 signal (37) through R1627 (1K/6). The circuit is powered by +12V and SYS_FAN_VCC. A large black arrow points from the top of the schematic to the bottom, indicating a connection to another part of the system.

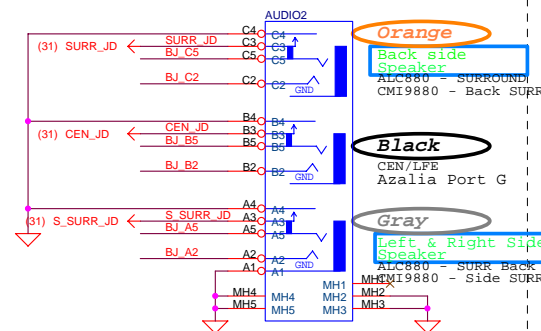
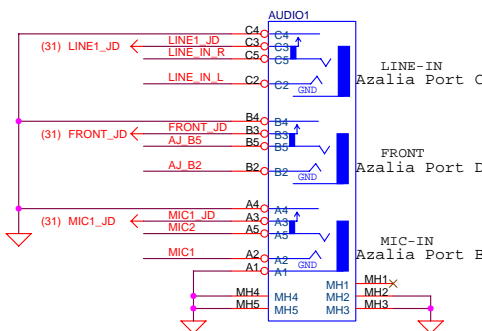
Title			
FAN CONTROL			
Size B	Document Number	8I945GMBX	Rev 1.0
Date:	Friday, July 01, 2005	Sheet	30 of 42



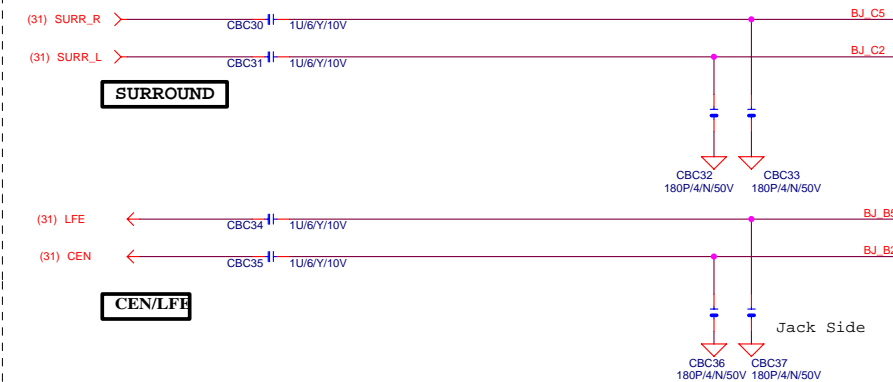
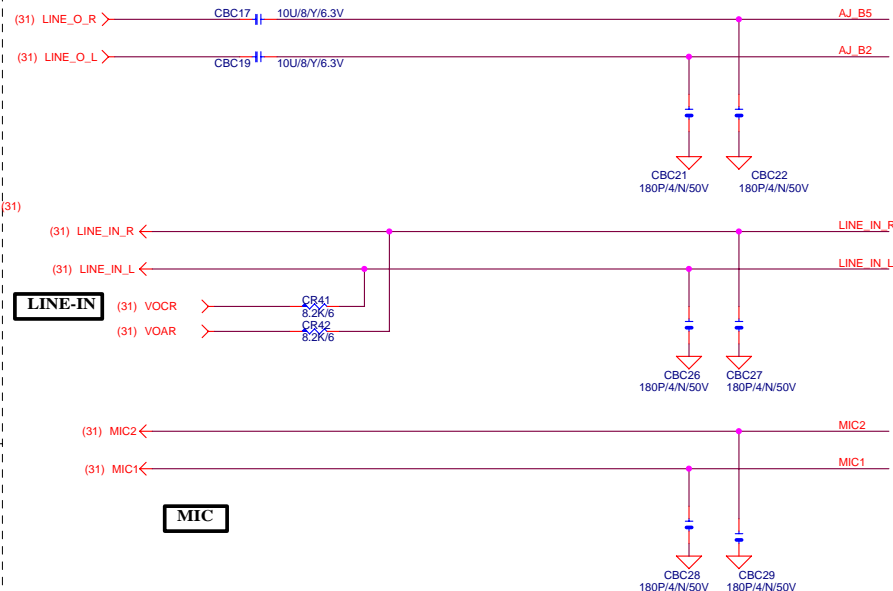


Azalia Jack
Normal --> pin4/pin3 open
Plug jack --> pin4/pin3 close

CMi9880 Port A is Side SURROUND, Port H is Back SURROUND
ALC880 Port A is SURROUND, Port H is SIDE



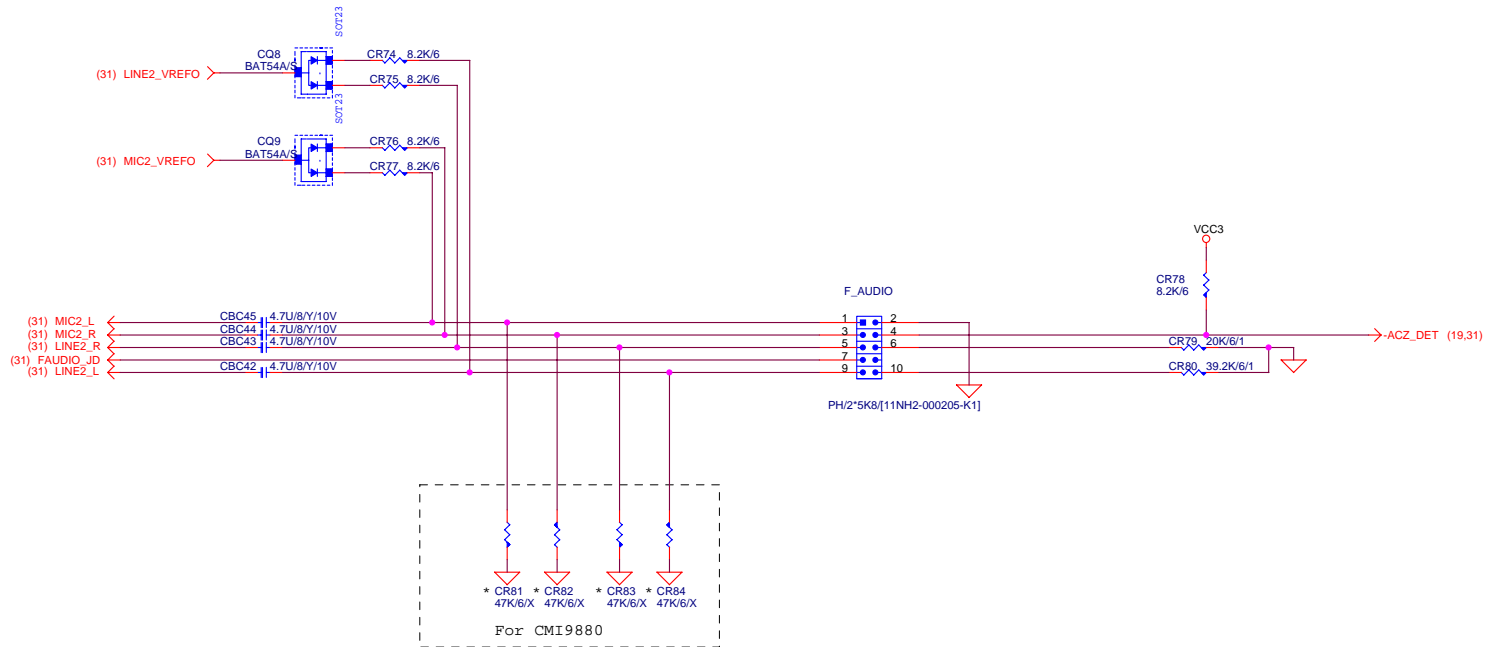
LINE OUT FRONT OUT



Intel Confidential			
Title			
AUDIO JACK			
8I945GMBX			
Size	Document Number	Rev	1.01
Custom			
Date:	Friday, July 01, 2005	Sheet	32 of 42

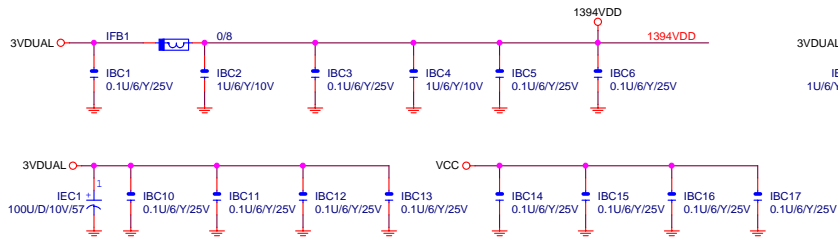
Azalia Port F

Azalia Port E



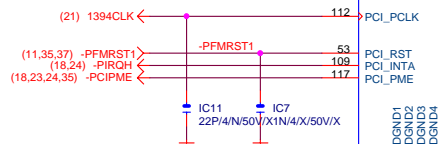
Intel Confidential

Title			
FRONT AUDIO CONNECTOR			
Size	Document Number	81945GMBX	Rev
Custom			1.01
Date:	Friday, July 01, 2005	Sheet	33 of 42

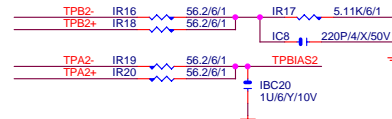
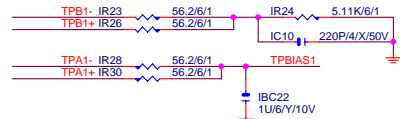
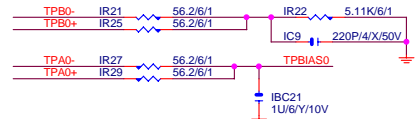


A D0	52	PCI_AD0
A D1	50	PCI_AD1
A D2	49	PCI_AD2
A D3	48	PCI_AD3
A D4	47	PCI_AD4
A D5	45	PCI_AD5
A D6	44	PCI_AD6
A D7	42	PCI_AD7
A D8	38	PCI_AD8
A D9	37	PCI_AD9
A D10	37	PCI_AD10
A D11	34	PCI_AD11
A D12	35	PCI_AD12
A D13	33	PCI_AD13
A D14	31	PCI_AD14
A D15	29	PCI_AD15
A D16	14	PCI_AD16
A D17	13	PCI_AD17
A D18	11	PCI_AD18
A D19	10	PCI_AD19
A D20	9	PCI_AD20
A D21	8	PCI_AD21
A D22	6	PCI_AD22
A D23	5	PCI_AD23
A D24	128	PCI_AD24
A D25	127	PCI_AD25
A D26	125	PCI_AD26
A D27	124	PCI_AD27
A D28	122	PCI_AD28
A D29	121	PCI_AD29
A D30	120	PCI_AD30
A D31	118	PCI_AD31

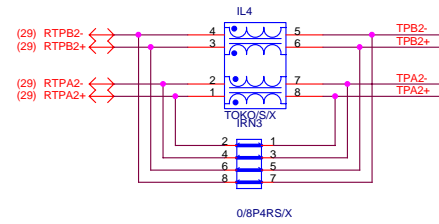
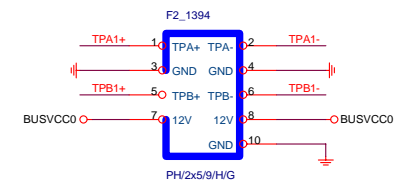
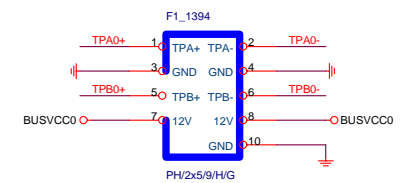
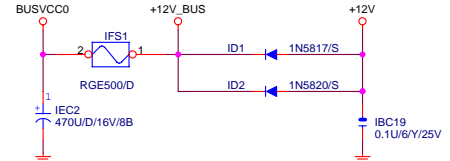
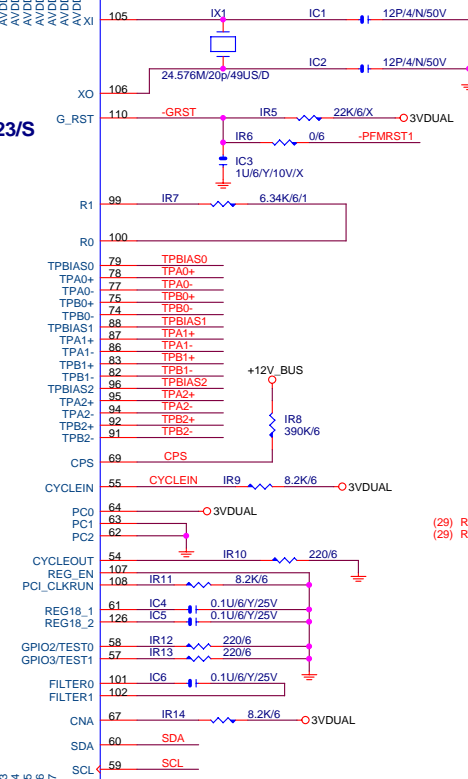
(18,24) -C_BE0	41	PCI_CBE0
(18,24) -C_BE1	15	PCI_CBE1
(18,24) -C_BE2	2	PCI_CBE2
(18,24) -C_BE3	2	PCI_CBE3
(18,24) PAR	26	PCI_PAR
(18,24) -FRAME	17	PCI_FRAME
(18,24) -IRDY	18	PCI_IRDY
(18,24) -TRDY	20	PCI_TRDY
(18,24) -DEVSEL	21	PCI_DEVSEL
(18,24) -STOP	22	PCI_STOP
(18,24) -STOP	4	PCI_IDSEL
(18,24) -REQ2	115	PCI_REQ
(18,24) -GNT2	114	PCI_GNT
(18,24) -PERR	24	PCI_PERR
(18,24) -SERR	25	PCI_SERR

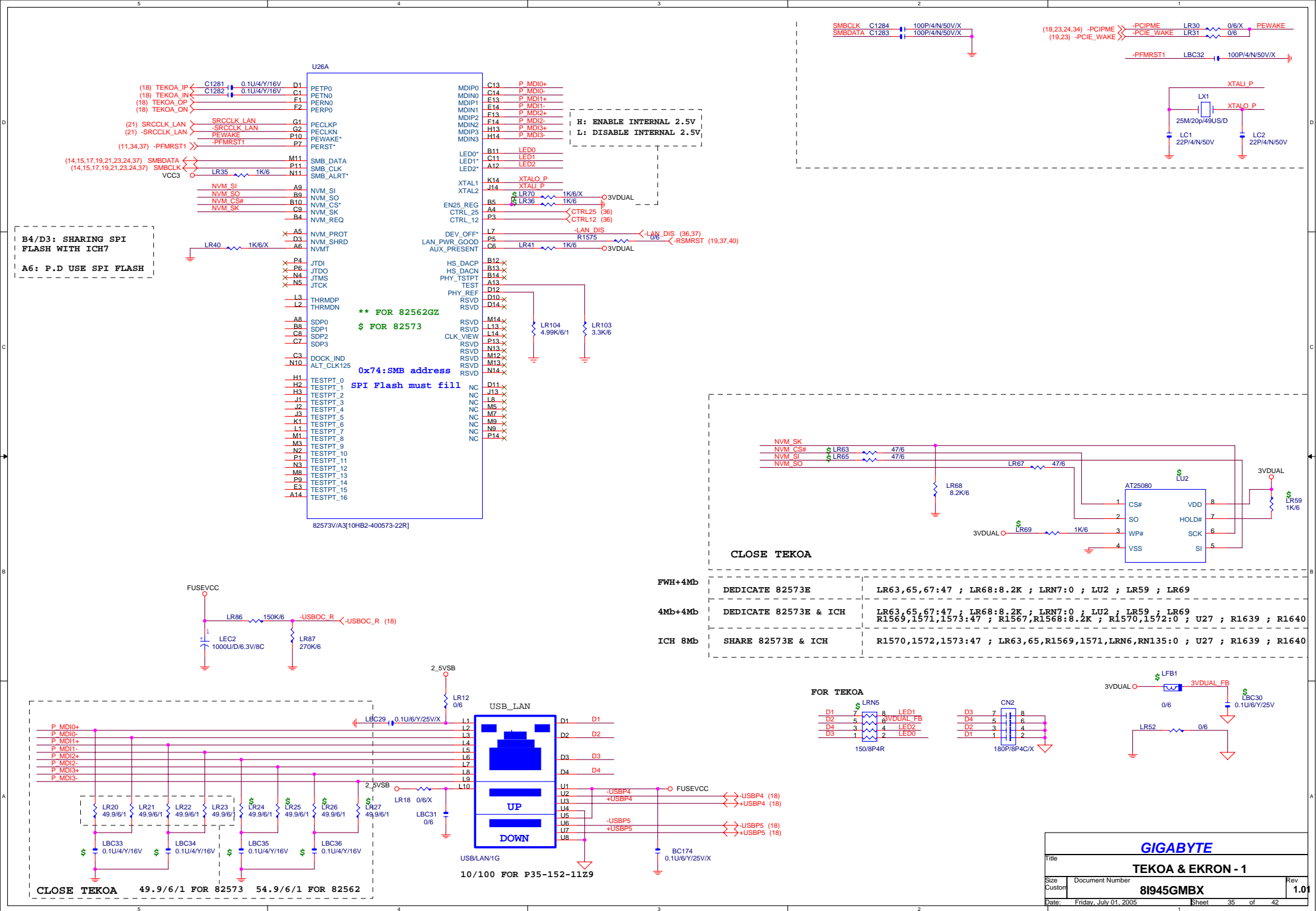


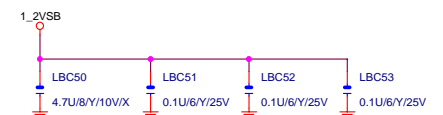
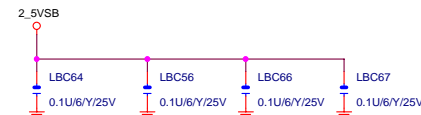
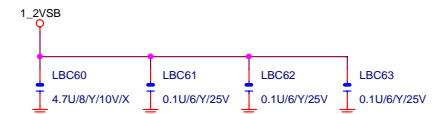
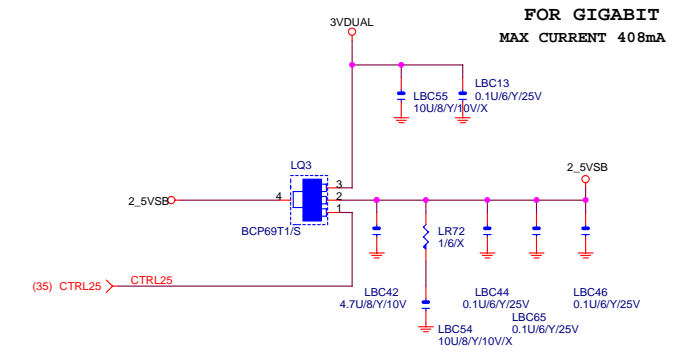
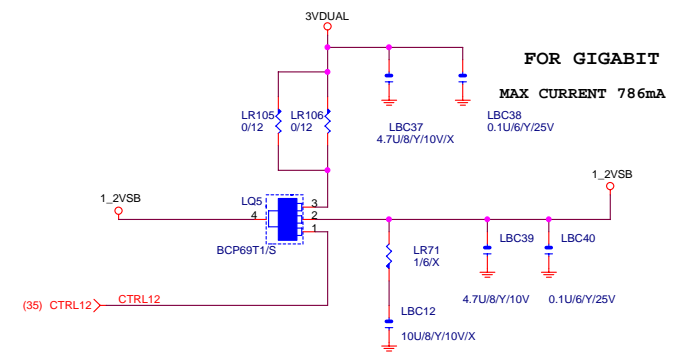
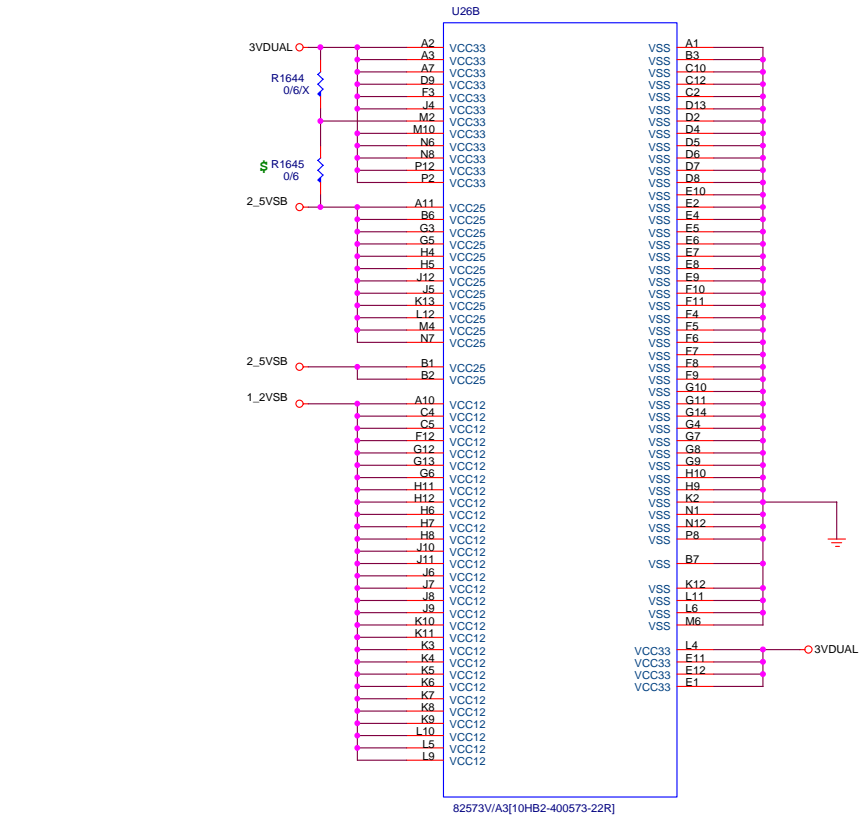
R1219 0/6 FOR ATMEL AT24C02N-10SI-2.7V
ATC ATC24LC02W

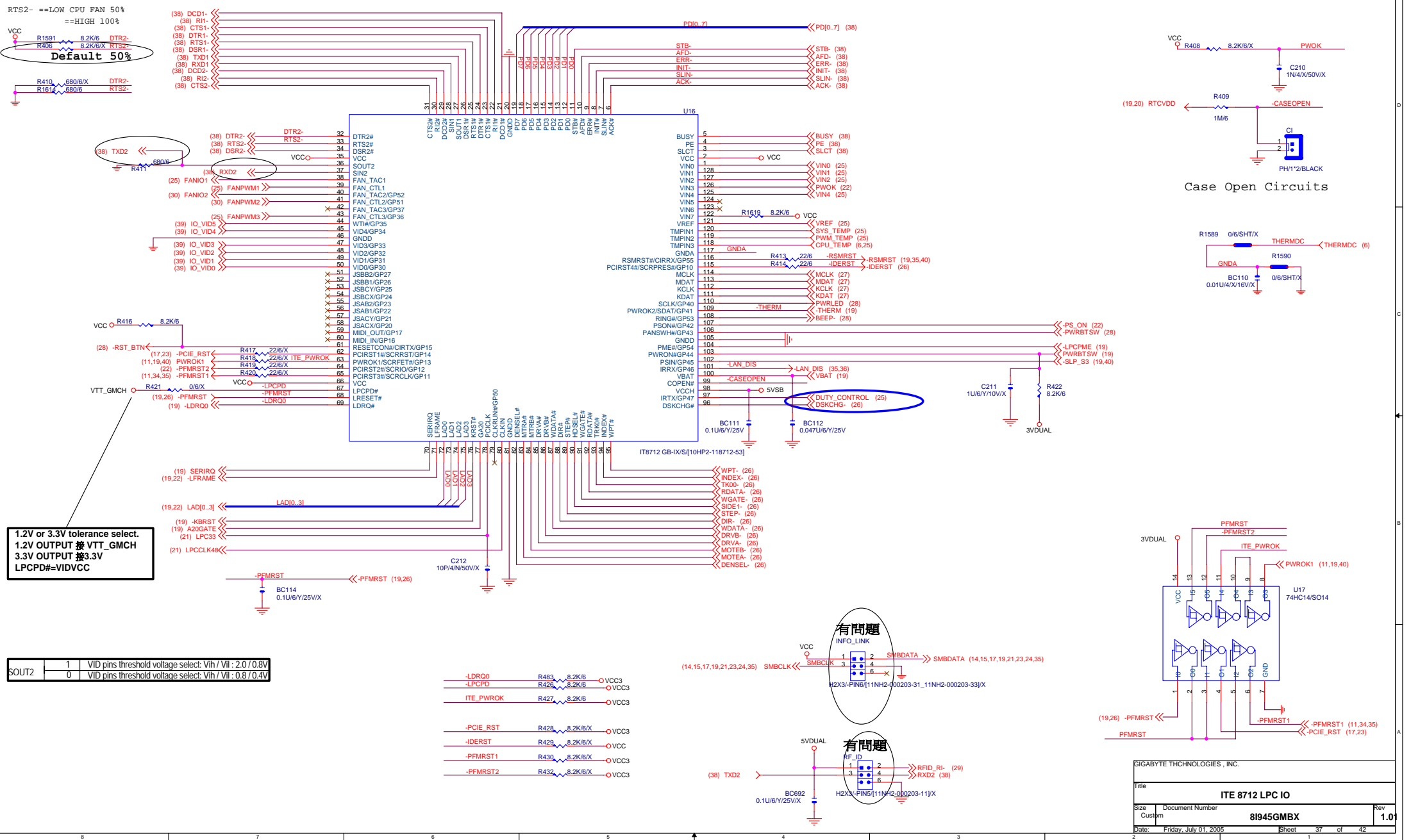


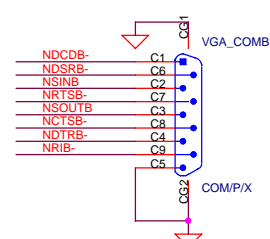
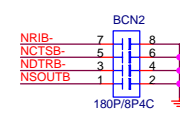
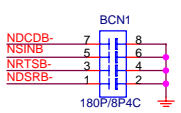
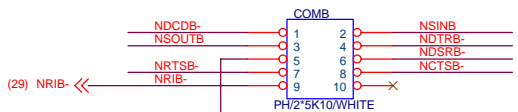
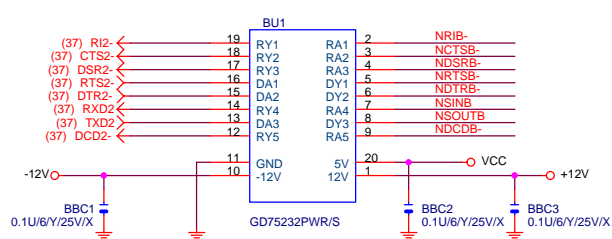
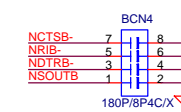
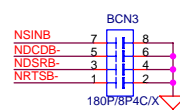
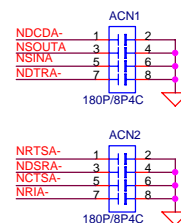
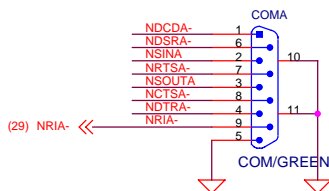
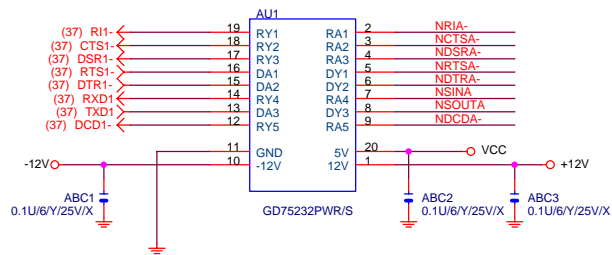
TSB43AB23/S





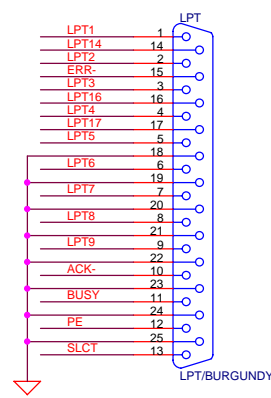
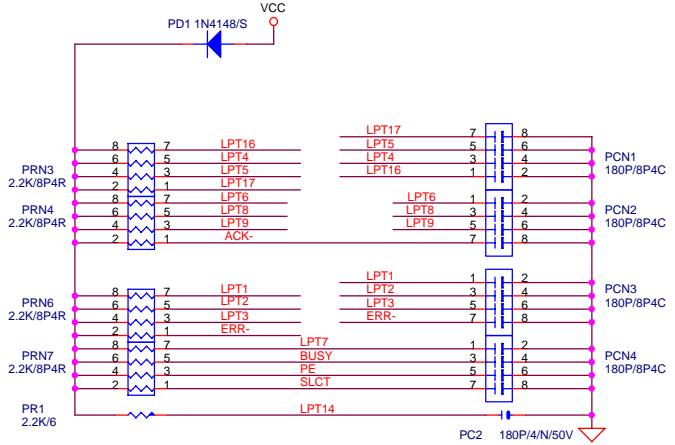
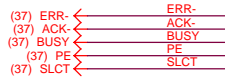
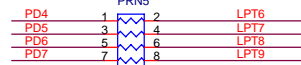
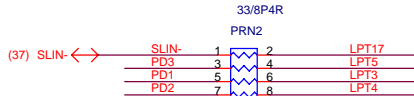
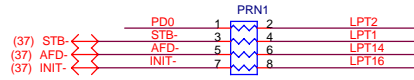




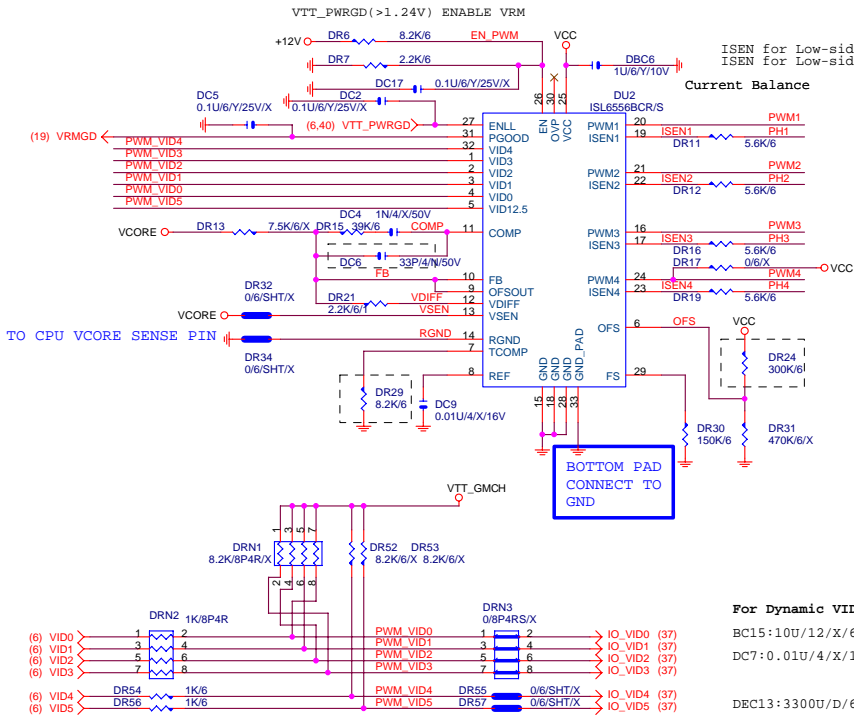
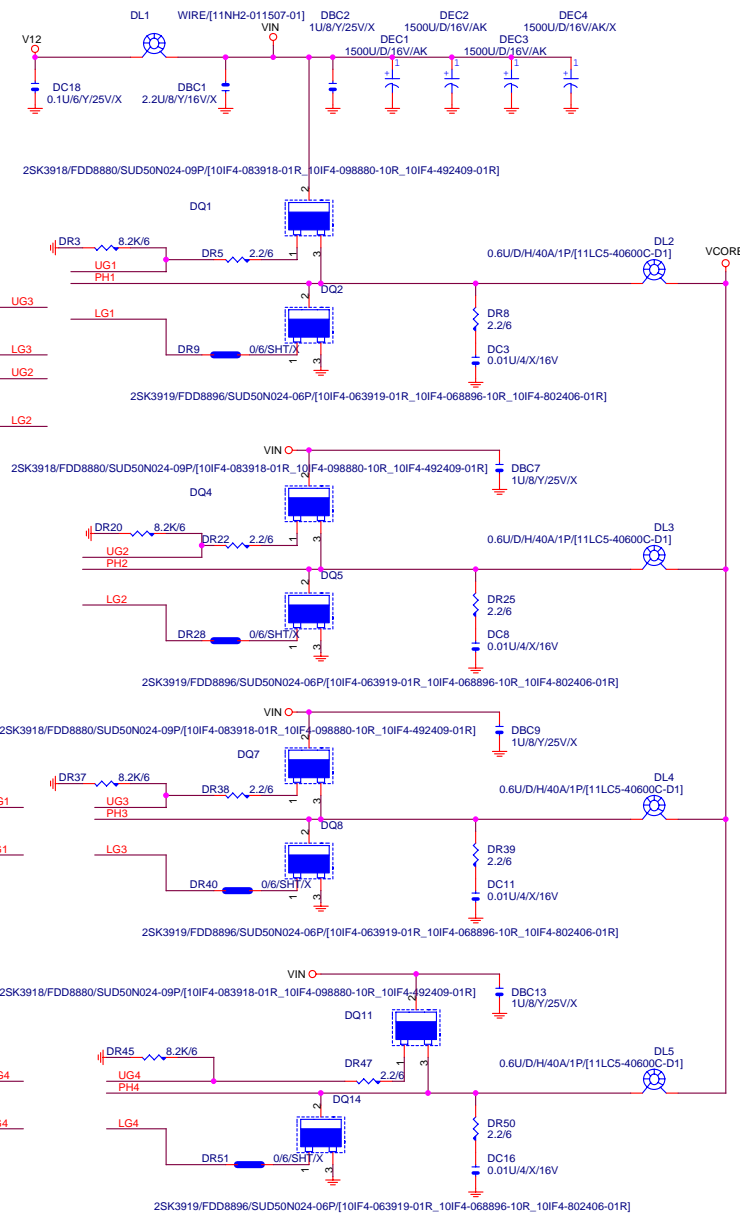
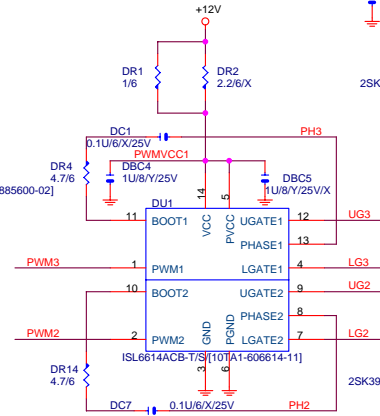
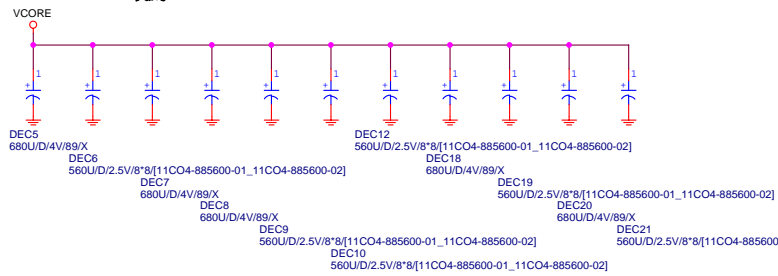


PLACE NEAR VGA_COM CONNECTOR

(37) PD[0..7] ↔ PD[0..7]



560uF改為8*8: 11C04-885600-01 & 02



For Dynamic VID Test: (93.07.12)

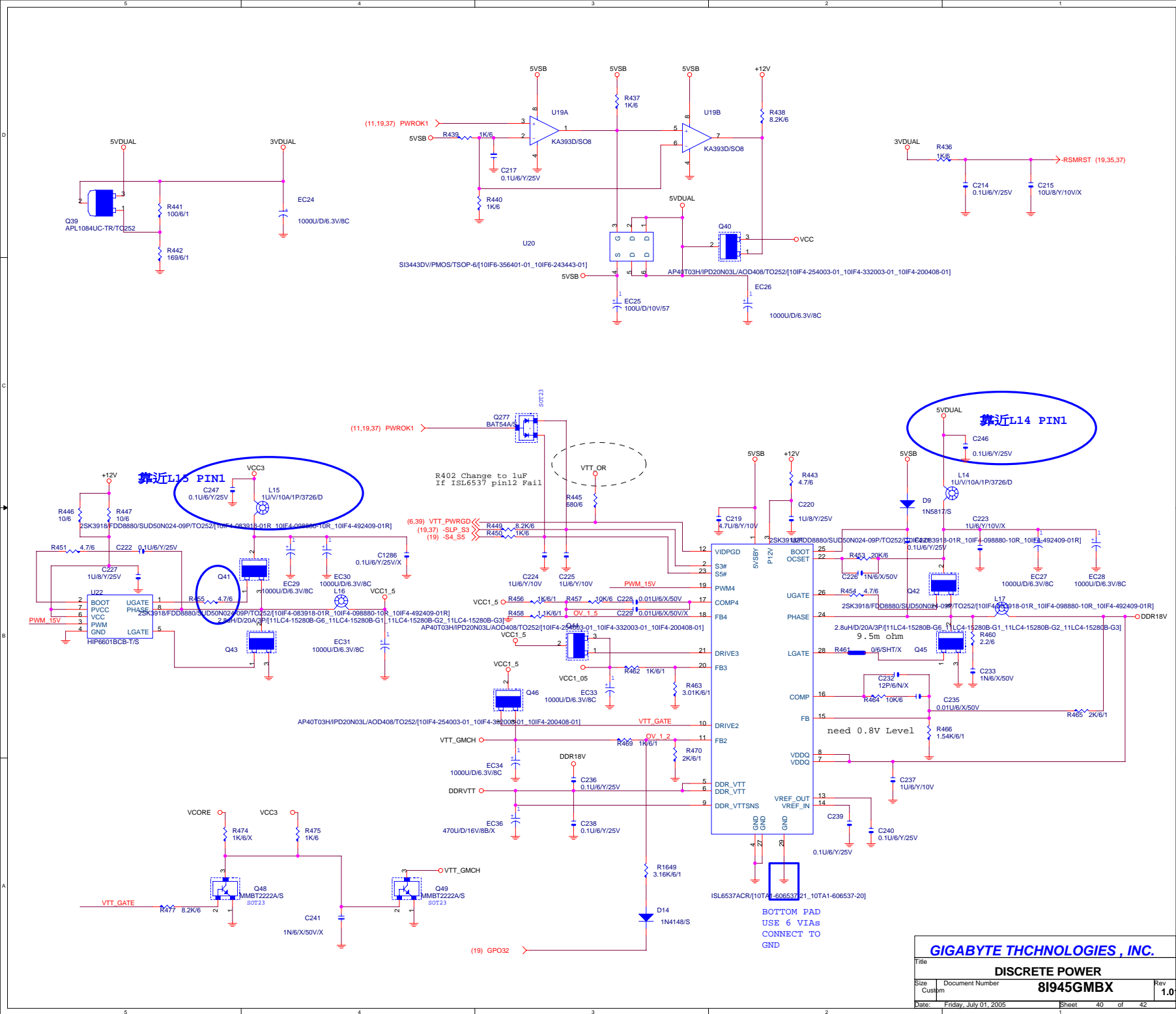
BC15:10U/12/X/6.3V-->22U/12/X/6.3V

DC7:0.01U/4/X/16V-->1000P/4/X/50V

DEC13:3300U/D/6.3V/AN-->1000U/D/6.3V/AC

DEC11:3300U/D/6.3V/AN-->N/A

Gigabyte Technology			
Title		VRD 10.1/ ISL6556	
Size	Document Number	81945GMBX	Rev
Custom			1.01
Date:	Friday, July 01, 2005	Sheet	39 of 42



INTEL ICH7 GPIO Implementation

紅字表示CPI/O 同PIN

GPI PIN

Pin Name	Pin Type	Power Well			GPIO Application
GPIO[0]	I/O	VCC3	GPI/BM_BUSY#	(NA)	(NA)
GPIO[1]	I/O	VCC	-REQ[5]	(P.U VCC)	-REQ[5]
GPIO[5:2]	I/OD	VCC	-PIRQ[H:E]	(P.U VCC)	-PIRQ[H:E]
GPIO[6]	I/O	VCC3	GPI	(NA)	M_ID0 FOR MEDIA
GPIO[7]	I/O	VCC3	GPI	(NA)	DUALBIOS_INPUT
GPIO[8]	I/O	3VDUAL	GPI	(P.U 3VDUAL)	-SKTOCC
GPIO[9]	I/O	3VDUAL	GPI	(NA)	P66DET
GPIO[10]	I/O	3VDUAL	GPI	(NA)	M_ID1 FOR MB_ID
GPIO[11]	I/O	3VDUAL	-SMBALERT	(P.U 3VDUAL)	-SMBALRT
GPIO[12]	I/O	3VDUAL	GPI	(NA)	M_ID2 FOR MB_ID
GPIO[13]	I/O	3VDUAL	GPI	(P.U 3VDUAL)	-LPCPME
GPIO[14]	I/O	3VDUAL	GPI	(NA)	M_ID3 FOR MB_ID
GPIO[15]	I/O	3VDUAL	GPI	(NA)	-ACZ_DET
GPIO[16]	I/O	VCC3	GPO	P.D 20K(INT.)	HW RESET
GPIO[17]	I/O	VCC3	GPO/-GNT[5]	(NA)	GPO/-GNT[5]
GPIO[18]	I/O	VCC3	GPO/toggle	(NA)	(NA)
GPIO[19]	I/O	VCC3	SATA1GP	(P.U VCC3)	SATA1GP
GPIO[20]	I/O	VCC3	GPO	(P.U VCC3)	TBL-
GPIO[21]	I/O	VCC3	SATA0GP	(P.U VCC3)	SATA0GP
GPIO[22]	I/O	VCC3	-REQ[4]	(P.U VCC)	-REQ[4]
GPIO[23]	I/O	VCC3	LDRQ1#	(NA)	(NA)
GPIO[24]	I/O	3VDUAL	GPO/reset not cleared	(NA)	(NA)
GPIO[25]	I/O	3VDUAL	GPO	(NA)	PWD_LED
GPIO[26]	I/O	3VDUAL	EL_RSVD	(P.D)	-SPI_WP
GPIO[27]	I/O	3VDUAL	EL_STATE0	(NA)	(NA)
GPIO[28]	I/O	3VDUAL	EL_STATE1	(NA)	(NA)
GPIO[29]	I/O	3VDUAL	OC5#	(P.U VCC 分壓)	OC5#
GPIO[30]	I/O	3VDUAL	OC6#	(P.U VCC 分壓)	OC6#
GPIO[31]	I/O	3VDUAL	OC7#	(P.U VCC 分壓)	OC7#
GPIO[32]	I/O	VCC3	GPO	(NA)	DUAL BIOS
GPIO[33]	I/O	VCC3	GPO	(NA)	DUAL BIOS
GPIO[34]	I/O	VCC3	GPO	(P.U VCC3)	FWP-
GPIO[35]	I/O	VCC3	SATACLKREQ#	(NA)	(NA)
GPIO[36]	I	VCC3	SATA2GP	(P.U VCC3)	SATA2GP
GPIO[37]	I	VCC3	SATA3GP	(P.U VCC3)	SATA3GP

GPO PIN

Pin Name	Pin Number	Power Well	Pin Type		GPIO Application
GPIO[38]	I/O	VCC3	GPI	(NA)	(NA)
GPIO[39]	I/O	VCC3	GPI	(NA)	(NA)
GPIO[40:47]			NOT IMPLEMENTED		NOT IMPLEMENTED
GPIO[48]	I/O	VCC3	-GNT[4]	(NA)	-GNT[4]
GPIO[49]	I/O	VTT_GMCH	CPUPWRGD	(P.U VTT_OL)	CPUPWROK
PC11	PCLK0	-PCIRST	-REQ0/-GNT0	-PIRQE	A_D16
PC12	PCLK1	-PCIRST	-REQ1/-GNT1	-PIROD	A_D17
PC13	PCLK2	-PCIRST	-REQ2/-GNT2	-PIROC	A_D18
1394b	1394CLK	-PFMRST2	-REQ3/-GNT3	-PIROH	A_D23
IT8212	RAIDCLK	-PFMRST2	-REQ4/-GNT4	-PIROG	A_D22

ICH6 GPIO Table:

NAME	PWR LANE	USAGE	NAME	PWR LANE	USAGE
GPI0	V5REF	M/B ID (-REQ6)	GPI41	VCC3	M/B ID
GPI1	V5REF	-REQ5	GPO48	VCC3	-GNT4
GPI2	V5REF	-PIRQE	GPO49	V-CPUIO	CPUPWOK
GPI3	V5REF	-PIRQF			
GPI4	V5REF	-PIRQG			
GPI5	V5REF	-PIRQH			
GPI6	VCC3	-SLP BTN			
GPI7	VCC3	DUAL BIOS			
GPI8	3VDAUL	-LANWAKE			
GPI9	3VDAUL	-USBOC4			
GPI10	3VDAUL	-USBOC5			
GPI11	3VDAUL	-SMBALT			
GPI12	VCC3	ATX DET			
GPI13	3VDAUL	-LPCPME			
GPI14	3VDAUL	-USBOC6			
GPI15	3VDAUL	-USBOC7			
GPO16	VCC3	CPU OV1 (-GNT6)			
GPO17	VCC3	-GNT5			
GPO18	VCC3	CPU OV2			
GPO19	VCC3	DUAL BIOS			
GPO20	VCC3	BIOS T-BLOCK			
GPO21	VCC3	DUAL BIOS			
GPO23	VCC3	DDR OV0			
GPI024	3VDAUL	GREEN LED			
GPI025	3VDAUL	DDR OV1			
GPI26	VCC3	SATA GP0			
GPI027	3VDAUL	+PWRLED			
GPI028	3VDAUL	-PWRLED			
GPI29	VCC3	SATA GP1			
GPI30	VCC3	SATA GP2			
GPI31	VCC3	SATA GP3			
GPI032	VCC3	BIOS WP			
GPI033	VCC3	AZALIA DET			
GPI034	VCC3	PWRLED			
GPI40	V5REF	-REQ4			

PWROK/RESET Table:

ITE8712BHX PIN	NET NAME	TARGET
PIN62/-PCIRST1	-PCIE_RST	1. PCI-E * 1 Slot1 2. PCI-E * 1 Slot2 3. PCI-E * 1 Slot3 4. PCI-E * 16 Slot
PIN64/-PCIRST2	-PFMRST2	1. Onboard PCI Lan 2. Onboard 1394 Chip 3. OnBoard FWH
PIN65/-PCIRST3	-PFMRST1	1. Onboard PCI-E Lan 2. Onboard SATA Chip 3. GMCH
PIN115/-PCIRST4	-PFMRST -IDERST	Reserved For IDE
PIN63/PWROK1	PWROK1	1. GMCH 2. ICH6 3. 5VDUAL SWITCH 4. DPS CONTROL
PIN109/PWROK2	-THERM	1. ICH6

GIGABYTE THCHNOLOGIES , INC.

Title		GPIO/RESET TABLE	
Size	Document Number	8I945GMBX	Rev
Custom			1.01
Date:	Friday, July 01, 2005	Sheet	42 of 42

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